NAVAL POSTGRADUATE SCHOOL
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THESIS

DESIGN, FABRICATION, AND ASSEMBLY OF A TEST PLATFORM FOR A HIGH-SPEED GaAs DRAM VLSI IC

by

Byron A. Ginter II

December, 1994

Thesis Advisor: Douglas J. Fouts

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ABSTRACT

The goal of this project is to redesign, fabricate, and assemble a digital circuit operating near a frequency of 250 MHz to test a new experimental Gallium Arsenide (GaAs) Dynamic Random Access Memory (DRAM). This thesis presents the redesigned six-layer printed circuit test fixture and the design of the DRAM hold down clamp necessary to affix the DRAM to the test fixture. The use of commercially available Computer Aided Design (CAD) and Computer Aided Manufacturing (CAM) tools were used for layout and fabrication. Finally, the assembly and testing of the test fixture, as well as problems encountered during the redesign, fabrication, and assembly processes, are discussed.

TABLE OF CONTENTS

I. INTRODUCTION

A. GaAs DRAM

The GaAs DRAM is a 32-bit memory consisting of eight address locations by four bits of information. It is packaged in a 132-pin Leaded Ceramic Chip Carrier (LDCC) utilizing surface mount technology (SMT). The GaAs DRAM pin assignments are shown in Table 1-1.

The GaAs DRAM signals are converted to Emitter Coupled Logic (ECL) voltage level at the I/O pads, making the chip appear to be an ECL for all practical purposes. The internal signals and interface parameters are shown in Table 1-2 [Ref. 2].

B. GENERAL DESIGN PARAMETERS

The final product of this thesis is a high speed printed circuit board which is to be used as a test platform for a Gallium Arsenide Dynamic Read/Write Memory (GaAs DRAM) chip. The GaAs DRAM was a product of previous research [Ref. 1] and has been simulated in HSPICE at a speed of 250 MHz. This high speed operation required that a special test platform be designed, and a preliminary printed circuit board design was completed in September 1993 [Ref. 2]. The basic ECL design was completed at that time, as was the simulation of the

board's operation using SUSIE-CAD, a WINDOWS© based schematic capture and logic simulation program.

TABLE 1-1 GaAs DRAM LDCC PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	NC	34	GND	67	NC	100	GND
2	RVREF	35	INCLK(I)	68	NC	101	NC
3	GND	36	NC	69	GND	102	NC
4	GND	37	GND	70	GND	103	GND
5	-2.0V	38	D0(I)	71	-2.0V	104	VSS
6	NC	39	NC	72	NC	105	NC
7	WRITE(I)	40	D1(I)	73	NC	106	VREFB
8	READ(I)	41	GND	74	-2.0V	107	GND
9	NC	42	GND	75	NC	108	GND
10	NC	43	-2.0V	76	NC	109	-2.0V
11	REFRESH(I)	44	NC	77	D0(O)	110	NC
12	NC	45	D2(I)	78	NC	111	VREFD
13	NC	46	NC	79	NC	112	NC
14	A2(I)	47	GND	80	D1(O)	113	GND
15	NC	48	D3(I)	81	NC	114	NC
16	GND	49	NC	82	GND	115	NC
17	SUB	50	A0(I)	83	-2.0V	116	NC
18	NC	51	NC	84	NC	117	NC
19	NC	52	GND	85	D2(O)	118	GND
20	GNC	53	DAS(I)	86	NC	119	DRDY(O)
21	NC	54	NC	87	NC	120	NC
22	NC	55	NC	88	D3(O)	121	MBSY(O)
23	GNC	56	GND	89	NC	122	GND
24	NC	57	GND	90	NC	123	GND
25	NC	58	-2.0V	91	NC	124	-2.0V
26	GND	59	NC	92	NC	125	NC
27	NC	60	NC	93	NC	126	GND
28	GND	61	NC	94	GND	127	NC
29	-2.0V	62	GND	95	-2.0V	128	GND
30	GND	63	NC	96	GND	129	-2.0V
31	NC	64	NC	97	NC	130	NC
32	A1(I)	65	GND	98	NC	131	GND
33	NC	66	NC	99	NC	132	-2.0V

TABLE 1-2 GaAs DRAM INTERNAL/INTERFACE SIGNAL PARAMETERS

DESIGNATION	USE	INTERNAL VOLTAGE LEVELS	DEPENDENCIES & INFO
A0:A2	Address Inputs	LOW 0.0 to 0.4 V HIGH 1.0 to 1.1 V	Δ Clock @ nominal 250 MHz Variable for test
D0:D3	Data Inputs	LOW 0.0 to 0.4 V HIGH 1.0 to 1.1 V	Δ Clock @ nominal 250 MHz Variable for test
DAS	Data Strobe	LOW 0.0 to 0.4 V HIGH 1.0 to 1.1 V	Negative edge strobes input data
INCLK	DRAM System Clock	0.0 to 0.7 V 50% Duty Cycle	Variable for test purposes simulator clock @ 250 MHz
VDD	Main Chip Positive Power Supply	-2.0 V	≅1.31 amps (simulated)
VSS	Negative Supply for Level Shift	-2.5 V	≅69 milliamps (simulated)
VRVREF	Receiver Pad Reference	.7 V	≅1.1 milliamp (simulated)
VREFD	Dummy Precharge Reference	.26 V	≅300 microamp (simulated)
VREFB	Bitline Precharge Reference	.7 V	≅5 milliamp (simulated)
READ	Read Command Signal	LOW .4 V HIGH 1.1 V	Test limits ≅ Access Time @ 3 nsec
WRITE	Write Command Signal	LOW 0.0 to 0.1 V HIGH 0.5 V	Test limits ≅ Access Time @ 3 nsec
REFRESH	Refresh Clock	LOW 0.4 V HIGH 1.1 V	25 KHz 10% Duty Cycle Pulse Signal
D0:D3	Data Outputs	LOW 0.0 to 0.1 V HIGH 0.5 V	
MBSY	Memory Busy	LOW 0 V HIGH 1.1 V	Asserted on Read/Write or Refresh
DRDY	Data Ready	LOW 0 V HIGH 1.1 V	Asserted on Read/Write or Refresh

The requirement for a special test board for the GaAs DRAM arose because of the 250 MHz clock speed at which it was designed to operate. Currently at the Naval Postgraduate School, DRAM test equipment operating in the 20 MHz range is available. Faster equipment, operating near 80 MHz, is commercially available but prohibitively expensive and still will not reach the desired speed of operation.

C. PRINTED CIRCUIT BOARD DESIGN

The process of developing new technology requires an iterative approach that consists of formulating an idea, generating a design, evaluating the design, and incorporating changes as required by the evaluation. Depending upon the complexity of the technology and ideas involved, this process may be relatively quick and painless or drawn-out and excruciating. The tools which are used play a large part in this process.

Computer Aided Design (CAD) has allowed a new approach to this process which enables the engineer to bypass many of the restrictions placed on electronic design in the past. This thesis project incorporates extensive use of CAD in the development process and discusses the difficulties encountered with modern, commercially available CAD tools.

The PC board fabrication process and commercial manufacturing concerns when using Computer Aided Manufacturing (CAM) tools is also addressed. CAM has permitted increased

complexity of design which has resulted in increased component densities and the necessity of using space saving technology such as Surface Mount Devices (SMD). The multi-layer circuit board, which was the final outcome of this project, uses SMD for most components, with the exception of several switches.

II. PRINTED CIRCUIT BOARD DESIGN

The purpose of this chapter will be to describe the design changes incorporated into the original printed circuit board (PCB) design [Ref. 2] completed by LCDR Michael Butler for his thesis.

A. DESIRED PRINTED CIRCUIT BOARD CHANGES

The engineering design changes to the PCB necessary to ensure proper chip mating and attachment were deemed 'desired' changes.

1. VLSI Clamp Holes

The first design change needed was the addition of four holes in the vicinity of the center of the PCB. These holes would allow the VLSI hold down clamp (described in Chapter III) to be attached to the PCB. This would allow non-destructive (not soldered) attachment of the GaAs DRAM chip to the testing board. Even distribution of force over the leads from the GaAs DRAM chip would require the holes to be placed symmetrically.

The placement of the holes in the PCB proved to be more difficult than first anticipated due to the multi - layer design. The six layer PCB has two high-speed signal layers, Mid1 and Mid2, crisscrossing the center of the board.

The first attempt at hole placement moved the high-speed signal paths out of the area in the center to allow symmetrical placement of the holes. This resulted in many hours of learning the intricate workings of TANGO PCB PLUS [Ref. 3], the CAD package originally used for the PCB layout. Although TANGO allowed the modifications, many signal lines and plated through holes (commonly known as vias) had to be modified to allow a symmetrical placement. This had a cumulative effect from the center of the board outward. Some vias could not be moved due to the chip density of the original design and the need to maintain a 10 mil tolerance.

After many hours of working on the redesign, it became apparent that either the board would have to be laid out from the beginning with the holes in place or the requirement for symmetrical placement would be relaxed. The decision was made to place the holes near the center without symmetry to minimize rerouting of signal lines. The holes were then placed as shown in Figure 2-1. This resulted in rerouting of 26 signal lines and no vias.

The true ground plane (Figure 2-2) had to be modified to ensure 30 mil clearance around each of the holes. This required that the hand drawn ground plane be deleted and redrawn.

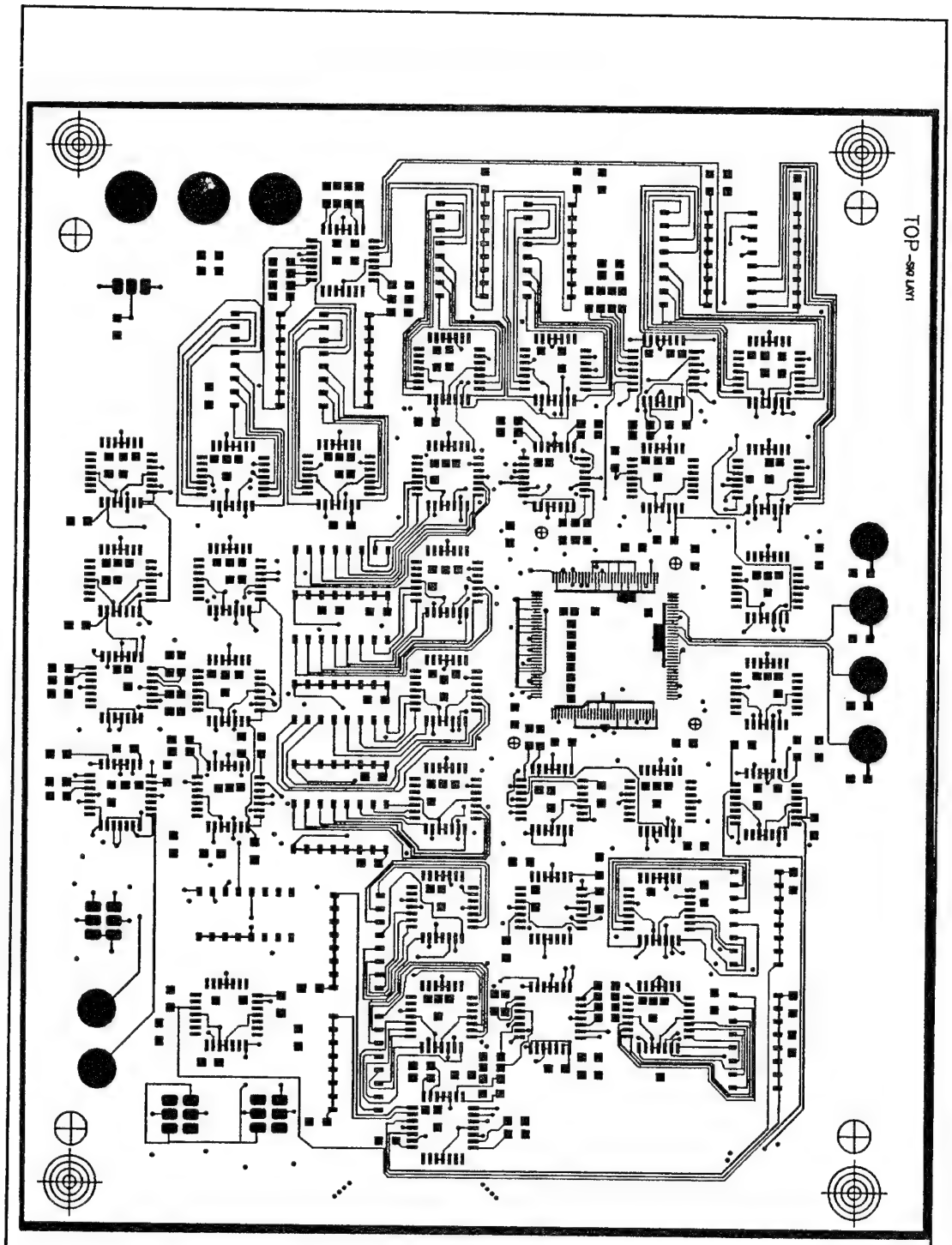

FIGURE 2-1. TOP LAYER SLOW SPEED SIGNAL AND PADS

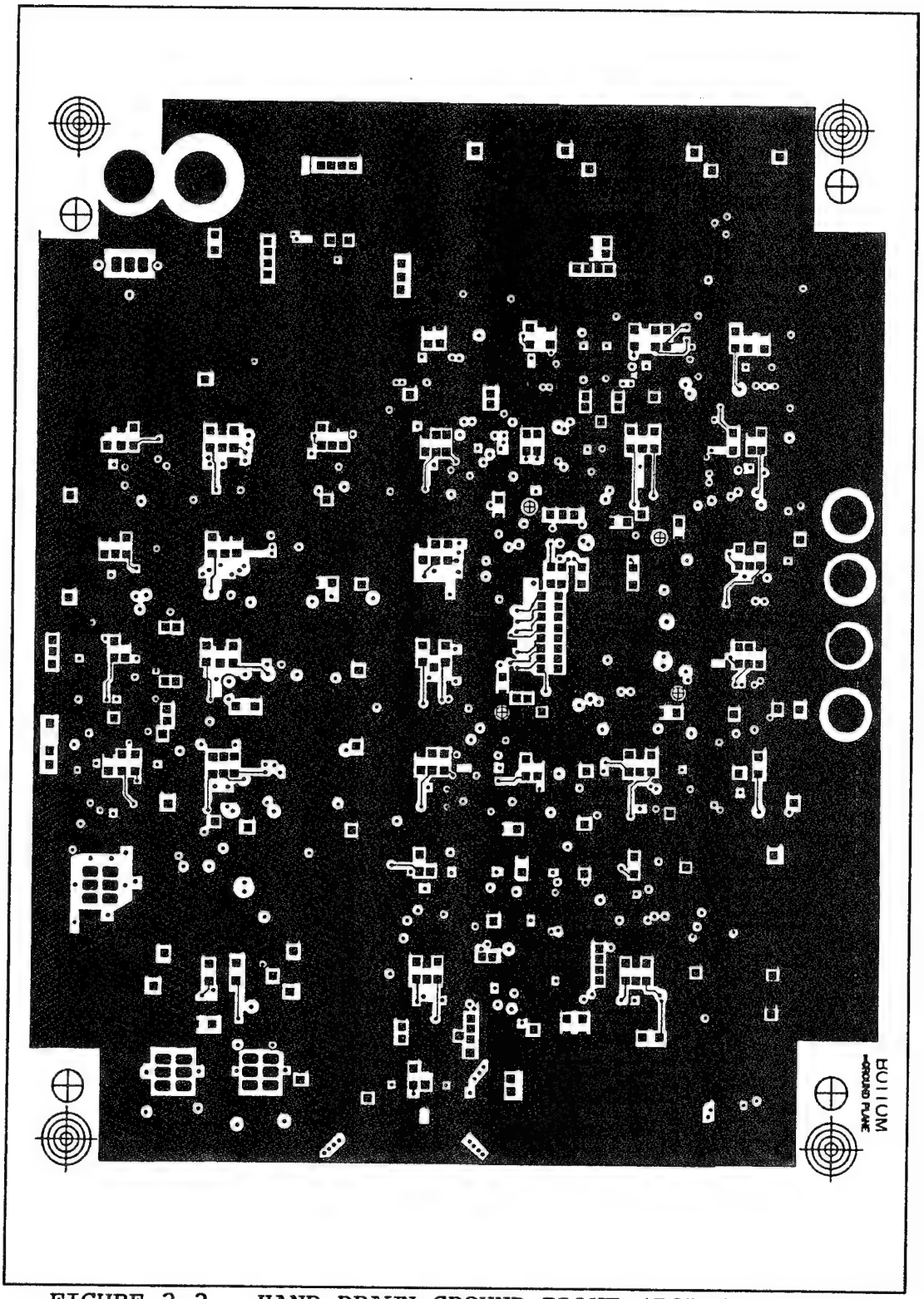

FIGURE 2-2. HAND DRAWN GROUND PLANE (BOTTOM LAYER)

2. Lengthening The GaAs DRAM Pads

To ensure proper mating between the GaAs DRAM chip and the test board, the pads on the PCB needed to be lengthened. The location of vias in the areas where the pads were located prevented making the pads as large as desired. Using the EDIT tool in TANGO PCB PLUS, the pads could be elongated symmetrically but not on one side only. This limited the increase in pad length to 15 mils for all but two pads. The two pads that could not be changed were between a via and the main pad run. Since the editing program within TANGO lengthened the pad equally on both sides, these two pads would have violated clearance allowances if enlarged. This was not considered to be a problem since the two pads in question had no signal lines attached. The pads are clearly visible in Figure 2-1 as the large square area near the center of the PCB.

B. REQUIRED PRINTED CIRCUIT BOARD CHANGES

Engineering design changes that were incorporated either to ensure producibility by the fabrication house or due to problems with TANGO PCB PLUS were deemed to be 'required' changes.

1. Board, Layer, And Dielectric Thickness

a. Loss Of Fabrication House

During the original design for the PCB in 1993, the fabrication house was contacted to ensure that the design met any specifications that were unique to the board house. Some examples include board thickness, minimum via size, and standard aperture tool settings.

After the desired engineering design changes were completed, it was learned that the original fabrication house had shut down. The new fabrication house, Western Circuit Technology, had several different requirements for the PCB fabrication. Most of these requirements did not alter the basic design; however, those which did alter the design proved to be difficult and time consuming to implement in TANGO PCB PLUS.

b. Design Considerations

The basic design consideration that changing the board, layer, and dielectric thickness affected was the requirement to maintain a constant characteristic impedance (Z_o) interconnect. The original design used an ECL standard Z_o of 50 Ω. The following design rules were adhered to [Ref. 2]:

1. Power requirements (labeling scheme depends on manufacturer):
    a. Most positive voltage equals ground (labeled VCC or GND).
    b. Most negative voltage in the range of -4.5 to -5.2 V (labeled as VEE).
    c. Voltage for termination resistor is -2.0 V (labeled as VBB/VTT).
2. The signal lines are terminated at the end with a resistor of 50 Ω. The signal line itself will have a geometry that supports 50 Ω impedance. One end of the terminating resistor will be connected as close as possible to the load input while the other end will be connected to -2.0 V.
3. Unused inputs/outputs are left unconnected. If an output is used, the associated complement terminal should be terminated.
4. The package is connected to VEE and VCC (GND). The end of the resistor (labeled TER) would be connected to the -2.0 V supply.

c. Effects Of Modifications On Z_o

Dielectric thickness was increased from 9 to 13 mils. Layer thickness was changed to 1 mil with 1 ounce copper. For six layers, this resulted in a total board thickness of 71 mils as compared to the original design thickness of 50 mils. The equation for Z_o from the *MECL System Design Handbook* [Ref. 4] is:

$$Z_o \doteq \frac{60}{\sqrt{E_r}} \times \ln\left[\frac{4 \times b}{|0.97 \times \times w \left(0.8+\frac{t}{w}\right)|}\right]$$

where E_r is the relative dielectric constant of the board material which is 5.0 for G-10 epoxy glass (FR4), w is the trace width (8 mils), t is the trace thickness which equals 1.4 mil for 1 ounce copper, and b is the ground plane to ground plane distance which equals 27 mils.

The final value for Z_o is 50.55 Ω as compared to the original design for which Z_o was 50 Ω by design of the specified layer, dielectric, and overall board thickness. This change is considered to be within tolerance for ECL design considerations.

2. Minimum Plated Through Hole Size

The original fabrication house had a via size of 15 mils. Western Circuit Technology, the new board house, required sizes no less than 16 mils. This seemed like a minor change at first; however, Tango PCB PLUS does not allow global edits to change all via sizes simultaneously. This required manual selection of each via for the subsequent size change.

The 464 vias in the PCB had to be individually checked and changed. This was a time consuming task which delayed sending the final photo plots to the fabrication house for a month. During this period, numerous problems experienced with the TANGO PCB PLUS software further delayed the final photo plots. These problems and their accompanying solutions will be discussed in the next section.

3. Required Changes Due To Problems With TANGO PCB PLUS

Numerous problems were encountered during the design and layout process. Some problems were encountered in the original board design files that were the starting point for this project. Some of the following errors were discovered after the proofs were submitted to the fabrication house. This necessitated fixing the problems and resubmitting the proofs. Cumulatively, these errors resulted in a four month delay in fabrication.

a. Hanging Traces

After proof submittal, two traces, one on the top layer and one on the Mid1 layer, were discovered to be incomplete runs. These incomplete runs did not appear as call outs from the TANGO PCB PLUS Design Rules Check software. After reviewing the original photo plot files, it was discovered that these incomplete runs were present in the original design. A careful tracing of the original schematic and corresponding photo plot revealed that the traces were extraneous and could be deleted. Attempts to delete these traces using TANGO PCB PLUS were unsuccessful.

After calling ACCEL's technical support personnel, the traces were deleted by manually editing the PCB source code. All photo plot proofs had to be regenerated after solving this problem.

b. Disconnected Signal Traces

After proof submittal, two traces on the top layer that had become disconnected were discovered. These traces were shown on the original proof submittal to the fabrication house as connected, yet during the course of revisions had become disconnected. This was disturbing from an engineering standpoint because no modifications had

been made to those particular nets. Furthermore, the error was not called out by the Design Rules Check software.

This necessitated a complete hand trace of all photo plots to ensure no further errors were present. One additional interrupted signal trace was discovered on the Mid2 layer. These problems were corrected, and all photo plots were regenerated.

c. Anti-Pad Swell

The vias which connect to the power and ground planes were required to 'swell' over the top layer specification by 30 mils. This would ensure proper connection to those internal layers.

The TANGO PCB PLUS software was supposed to accomplish this by the aperture tools settings that were established when the vias were laid down or edited. This was a completely separate problem from the minimum via size mentioned earlier. The problem was traced to the settings that were used during the original layout.

Two apertures are available for the pad during definition. The first is a 'flash' aperture which allows the shutter on the photo plotter to open briefly while the film remains stationary. The PCB

software does not 'swell' when a flash aperture is used. The second type of aperture is a 'draw' aperture. This allows the shutter on the photo plotter to remain open as the film is moved to draw the image of the pad on the film. When a 'draw' aperture is specified, the pad's power/ground swell setting enlarges the pad size when generating the photo plot for the power or ground plane. This ensures proper connectivity between the pad's via and the associated plane.

The corrective action for this problem required each pad with connections to the power or ground plane to be edited and the aperture changed from 'flash' to 'draw'. The photo plot files had to be regenerated following this correction.

d. Drill Drawing Legend

The fabrication house required a drill drawing file to be generated for the PCB manufacture. This was not one of the original design files. The TANGO PCB PLUS software automatically generates a file consisting of all holes that are to be drilled into the PCB. This file consists of different drill symbols for each size hole.

The software had no provision for generating a legend identifying the different symbols to the corresponding hole sizes on the drill drawing. A manually generated legend was created and faxed to the fabrication house to correct the problem.

e. Shorted And Open Circuits

Two layers generated by TANGO PCB PLUS would have generated short or open circuits on the top and bottom layers. The silk screen layers generated for the top and bottom layers would have printed over the component pads that were to be laid down. This would have resulted in an open circuit. This problem was found in the original design. The high circuit densities that were designed into the PCB made the silk screen layer overlap the circuit pads. This problem was corrected by the fabrication house by 'blowing out' any printing that would overlap a pad. This resulted in some of the printing on the PCB being illegible; however, the photo plot proofs can be used during assembly to identify component designators where necessary.

The solder masks for the top and bottom layers presented another problem. These masks are automatically generated by TANGO PCB PLUS from the completed design. The clearance that the software

used to generate the solder mask for both layers was properly set but the generated photo plots would allow overlap between adjacent pads causing short circuits on the completed designs. The built in Design Rules Check software for TANGO PCB PLUS did not identify either of these problems and would have allowed a faulty design to be manufactured. The fabrication house uses a more sophisticated design rule checker on all incoming photo plot files to spot problems before the expensive photo plots are generated. The fabrication house was able to adjust the solder mask tolerances correctly after authorization to modify the photo plot files.

f. Pads And Signal Lines Not Connected

The PCB I/O pads were found to be disconnected from their respective signal lines by the fabrication house. This problem was not identified by the Design Rules Check software or the built-in net checker. The result would have been a non-functional design. The fabrication house used their software to correct the problem after authorization for the modifications was given. The problem could not be corrected on the photo plot files generated by TANGO PCB PLUS as it showed the pads and signal lines being connected, when they were not.

C. VLSI TEST FIXTURE CLAMP

The need to connect the GaAs DRAM Chip to the PCB non-destructively led to the design of a special clamp (Figure 2-3) using AUTOCAD [Ref. 5].

The VLSI hold down clamp was laid out using AUTOCAD, Release 11, by constructing an AUTOCAD Interchange Format (DXF) file from the four holes laid out in TANGO PCB PLUS for the clamp. Importing this file into AUTOCAD, the structure for the clamp was laid out using the four holes as a template. A schematic was given to the Department of Mechanical Engineering for construction of the clamp. It was decided to use nylon as a base material to minimize interaction with the 250 MHZ clock used in the test platform. The clamp as constructed is shown in Figure 2-4.

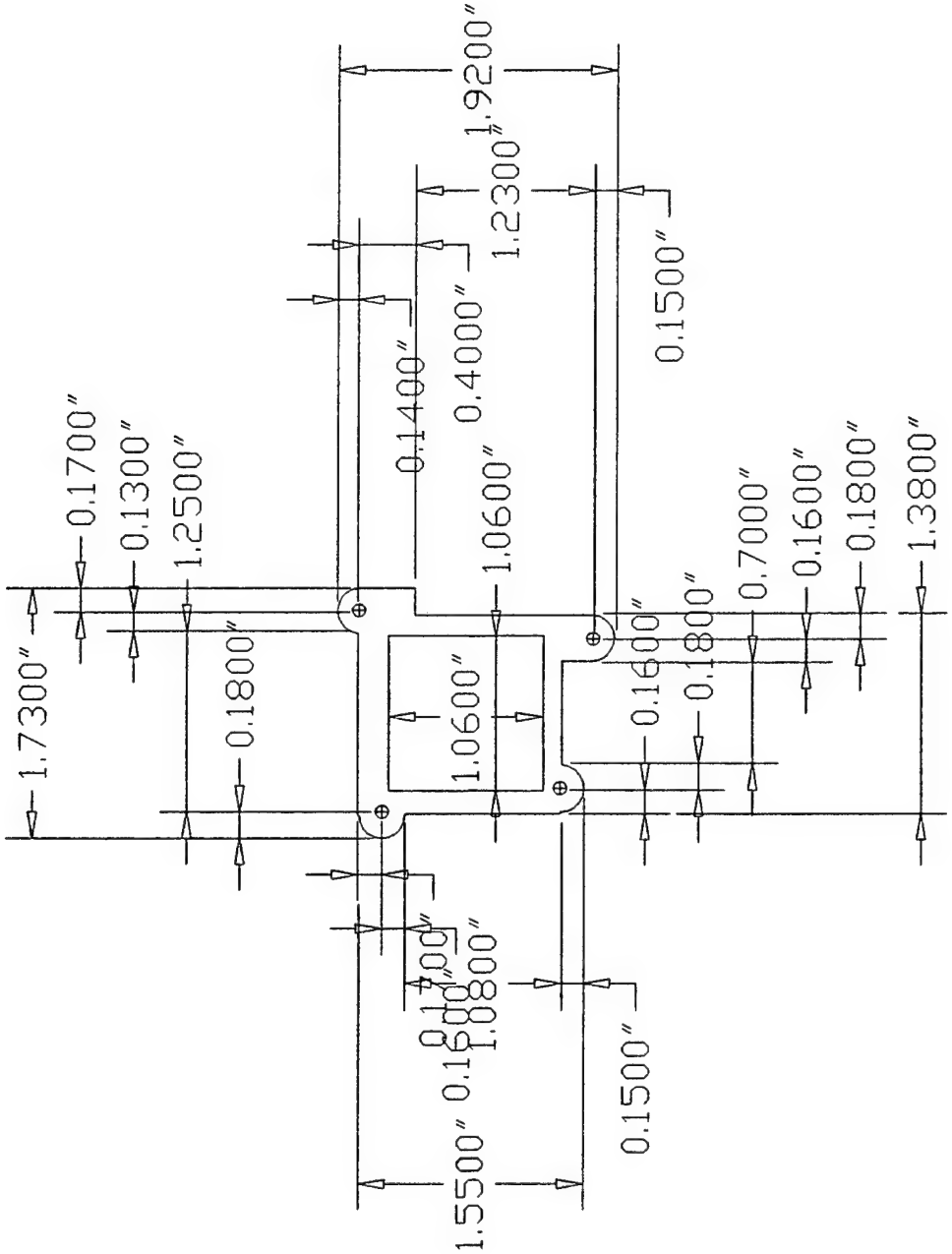

FIGURE 2-3 VLSI HOLD DOWN CLAMP SCHEMATIC

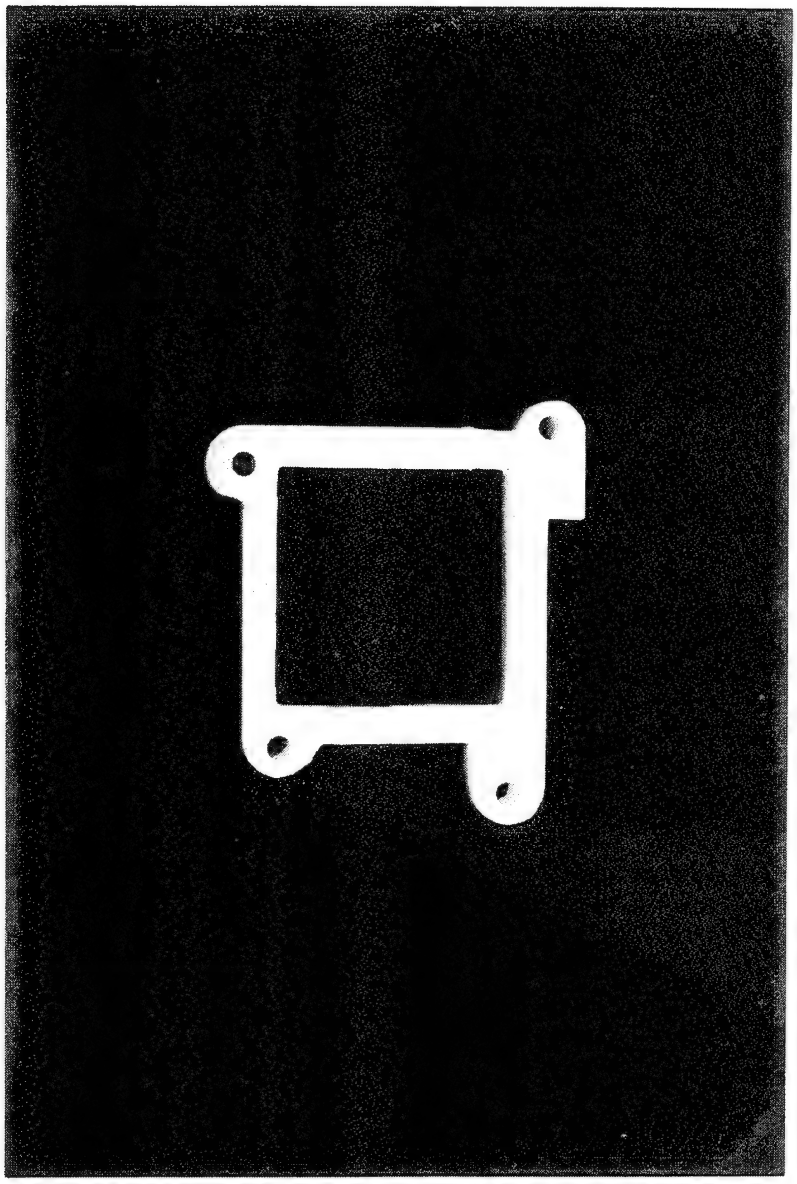

FIGURE 2-4 MANUFACTURED VLSI HOLD DOWN CLAMP

III. PRINTED CIRCUIT BOARD ASSEMBLY

A. PCB RECEIPT AND INSPECTION

Three PCB's, with the final photo plots, were received in late October from the fabrication house. An inspection was conducted on the printed circuit board prior to assembly. The PCB was compared to the photo plot files sent to the fabrication house. All signal lines, plated through holes, and non-plated through holes were checked. Since the board is a multi-layer design, only the top and bottom layers could be examined. The only errors found were J1 and J2, the external reset and clock in jacks. These were originally designed to be plated through holes but appeared as large pads on the final PCB. The photo plot files for the top layer showed J1 and J2 as pads, so the error was not due to the fabrication house.

Since all signals to J1 and J2 appear on the top layer, the problem can be alleviated by soldering jack connectors onto the PCB. No other problems have been identified with the final product. The PCB is shown in Figures 3-1 and 3-2.

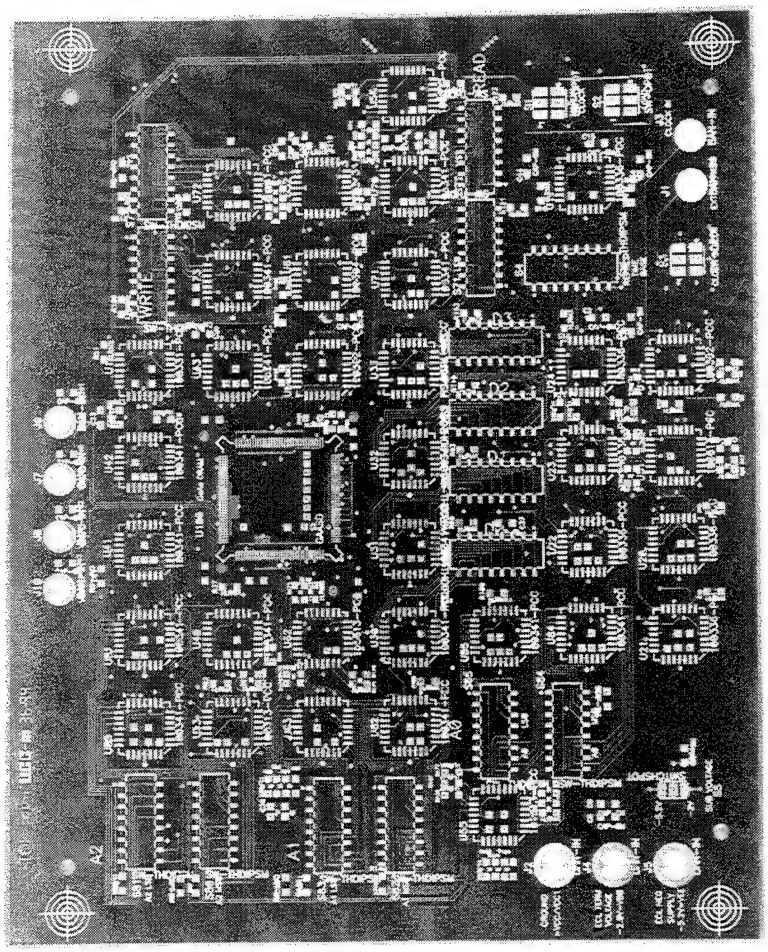

FIGURE 3-1 PRINTED CIRCUIT BOARD (TOP VIEW)

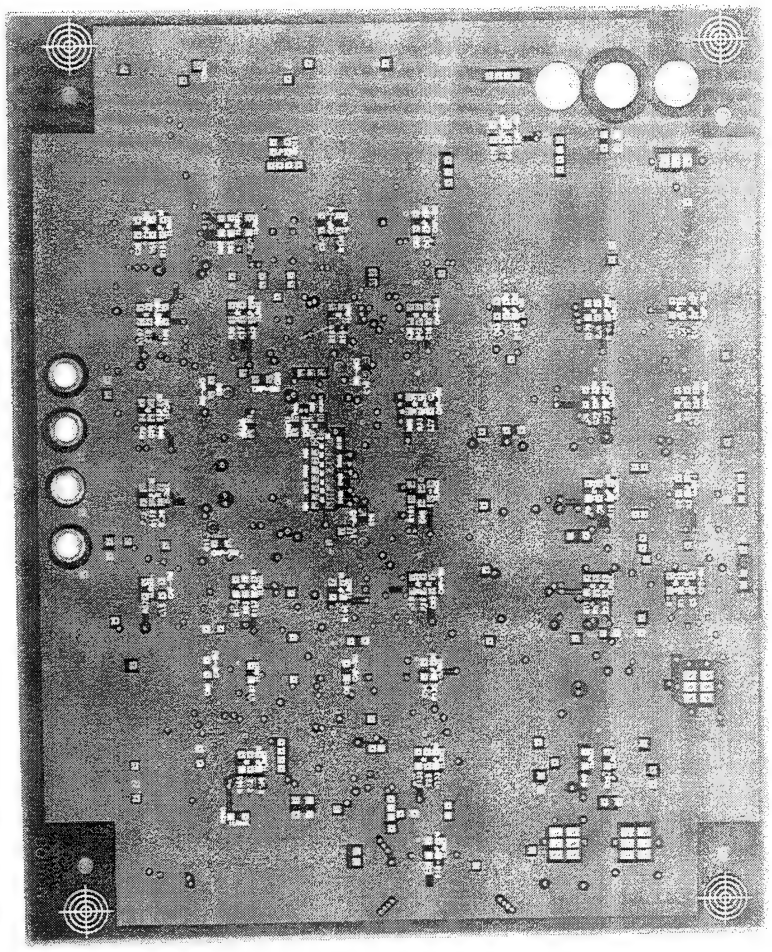

FIGURE 3-2 PRINTED CIRCUIT BOARD (BOTTOM VIEW)

B. ASSEMBLY

The task of assembling the test platform began with obtaining the required components as specified on the Bill of Materials (Appendix B). The ECL chips, resistors, and capacitors had been obtained before the start of the redesign. Only the surface mount dip, DPDT, and SPDT switches had to be procured. However, the commonly used sources to obtain components did not stock surface mount dip switches. After conferring with LCDR Butler, who completed the original design, an alternate source for these parts was identified. Because the DPDT and SPDT switches matching the footprints used on the PCB could not be obtained, the leads on the smallest commercially available switches were cut and bent to fit the designed footprint.

During the assembly process, a 700°F soldering iron was used. Two types of solder, paste and solid rosin core, were used depending on the type of component being installed. This was a time consuming process as there were 1651 solder connections on the PCB. Using high reliability soldering techniques (Appendix D), each joint was soldered, quenched with alcohol, cleaned, polished and inspected for surface defects. Experience has shown that applying the paste solder carefully to the SMD component leads, positioning the

component on the board, and then applying heat yielded the best results.

After all components were soldered in place, the power and signal jacks were bolted to the board. The completely assembled test platform is shown in Figures 3-3 and 3-4.

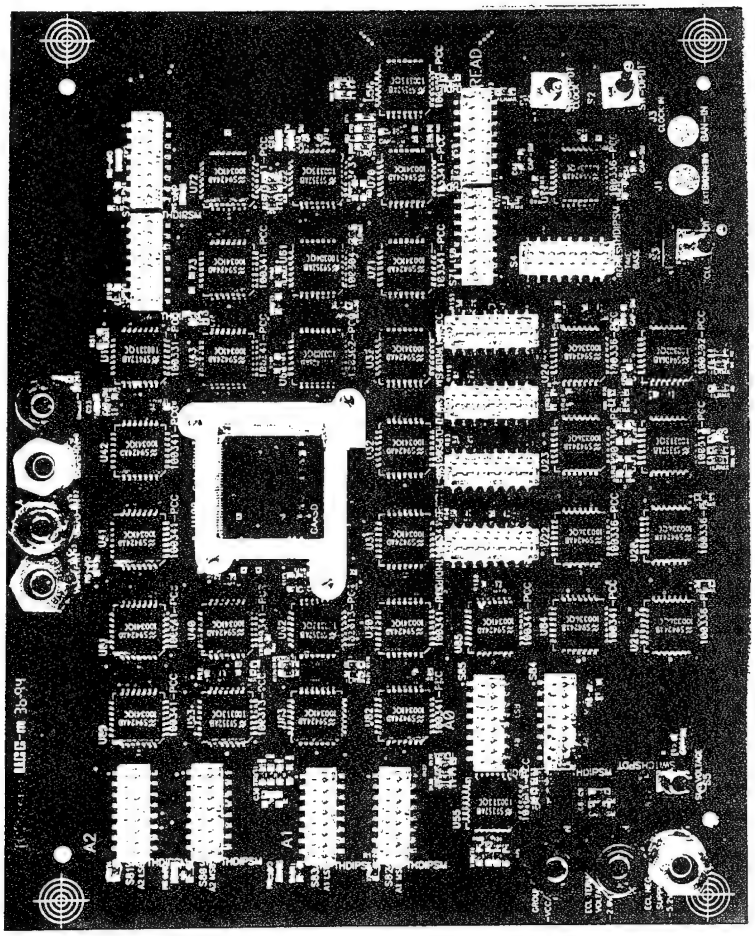

FIGURE 3-3 ASSEMBLED PRINTED CIRCUIT BOARD (TOP VIEW)

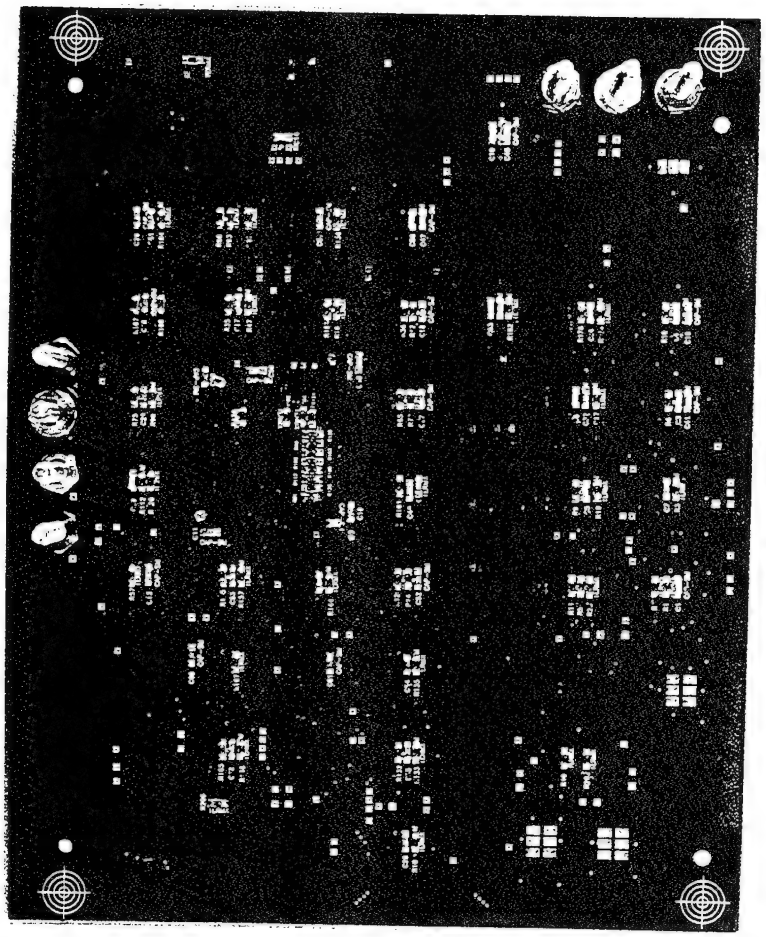

FIGURE 3-4 ASSEMBLED PRINTED CIRCUIT BOARD (BOTTOM VIEW)

IV. CONCLUSIONS

A. THE SCOPE OF THE PROJECT

Initially, this project was to pick up where the previous thesis had left off. Very little design was to be accomplished as the previous work should have encompassed all of the design necessary to bring the PCB to fabrication. With the closure of the original fabrication house, it became necessary to redesign the layout of the PCB. Close cooperation with the fabrication house throughout this project was required. Although no logic design changes were needed, the project became an iterative process of correcting problems with the photo plots, sending the photo plot files to the fabrication house, and learning of new problems that had to be corrected before the PCB could proceed to fabrication. The large, time consuming task of verifying photo plot proofs after every change could have been done better by a machine with properly operating checking tools.

The fabrication house recommended that future complex layouts be accomplished on a more robust software package. Their experiences with PCB design has shown that the majority of problems with designs submitted to them for fabrication are with early generation CAD/CAM packages. Currently, the Department of Electrical Engineering does not have a new generation PCB design package on line, but one is being loaded

into the computers. This should prevent problems in the future for similar complex PCB designs.

B. RECOMMENDATIONS

There were several problems encountered during this project that could have been easily prevented. The Bill of Materials that is generated by a software package does not provide a useable footprint for specific components. The designer should ensure that a separate listing is generated that shows the specific catalog and part numbers for each component listed. This would allow follow-on work to proceed much quicker as research to locate acceptably sized components would be eliminated.

The loss of the original fabrication house, although unique, is another point that needs to be addressed. The design changes to the PCB that were required by changing fabrication houses after design completion probably should have driven an entirely new layout due to the poor editing capabilities of TANGO PCB PLUS. This would have prevented many of the problems that were encountered during the iterative design change process. In the future, this may not be a problem if a more robust software package is used for PCB layout.

C. LAYOUT FOR BOARD ASSEMBLY

The high component density required for this project dictated the need to use surface-mount components, while budget constraints dictated a maximum board size. The resulting design was a nightmare to assemble by hand. This was noted by the previous designer but could not be altered due to the constraints. Human factors must be considered in any design that is to be assembled by hand. The component spacing on the PCB could have easily led to damage during the assembly process. Until the testing of the PCB is completed, damage to components will remain unknown. The level of skill required is probably beyond the average student's capabilities. As a former Electronics Technician, with high reliability soldering training, I found the task to be far more challenging than any for which I had been trained or experienced in the field.

D. OPERABILITY

It remains to be seen if the final PCB design will accomplish its intended function, testing the GaAs DRAM Chip. The potential exists that the board will not function as designed or that an error in the fabrication process resulted in a faulty PCB.

The other factor is that the GaAs DRAM Chip design may be faulty or was manufactured incorrectly. These questions will be answered by the testing process which is now ready to begin.

Great care was taken during the design and assembly process to ensure a properly operating test platform. The PCB has been checked at each step of the process and should operate as designed. Hopefully, the testing phase will provide useful data on the GaAs DRAM Chip which will increase the knowledge base for new designs.

APPENDIX A

This section contains the photo plot proofs for the printed circuit board as manufactured. Note that both the POWER (VBB termination voltage) and GROUND (VEE reference voltage) planes are plotted in the negative due to the software constraints. The BOTTOM layer which is the true GROUND plane is plotted in positive. The layers are labeled in order of their position as follows:

- Figure A-1 TOP ASSEMBLY LAYER
- Figure A-2 TOP SOLDER MASK
- Figure A-3 DRILL DRAWING
- Figure A-4 HOLES AND VIAS PLOT
- Figure A-5 TOP SILK SCREEN
- Figure A-6 TOP LAYER PADS AND SLOW SPEED SIGNAL
- Figure A-7 POWER = VBB TERMINATION (NEGATIVE)
- Figure A-8 LAYER Mid1 = FIRST FAST SIGNAL LAYER
- Figure A-9 GROUND = VEE LAYER (NEGATIVE)
- Figure A-10 LAYER MID2 = SECOND FAST SIGNAL LAYER
- Figure A-11 BOTTOM LAYER = TRUE GROUND PLANE
- Figure A-12 BOTTOM ASSEMBLY LAYER
- Figure A-13 BOTTOM SOLDER MASK
- Figure A-14 BOTTOM SILK SCREEN

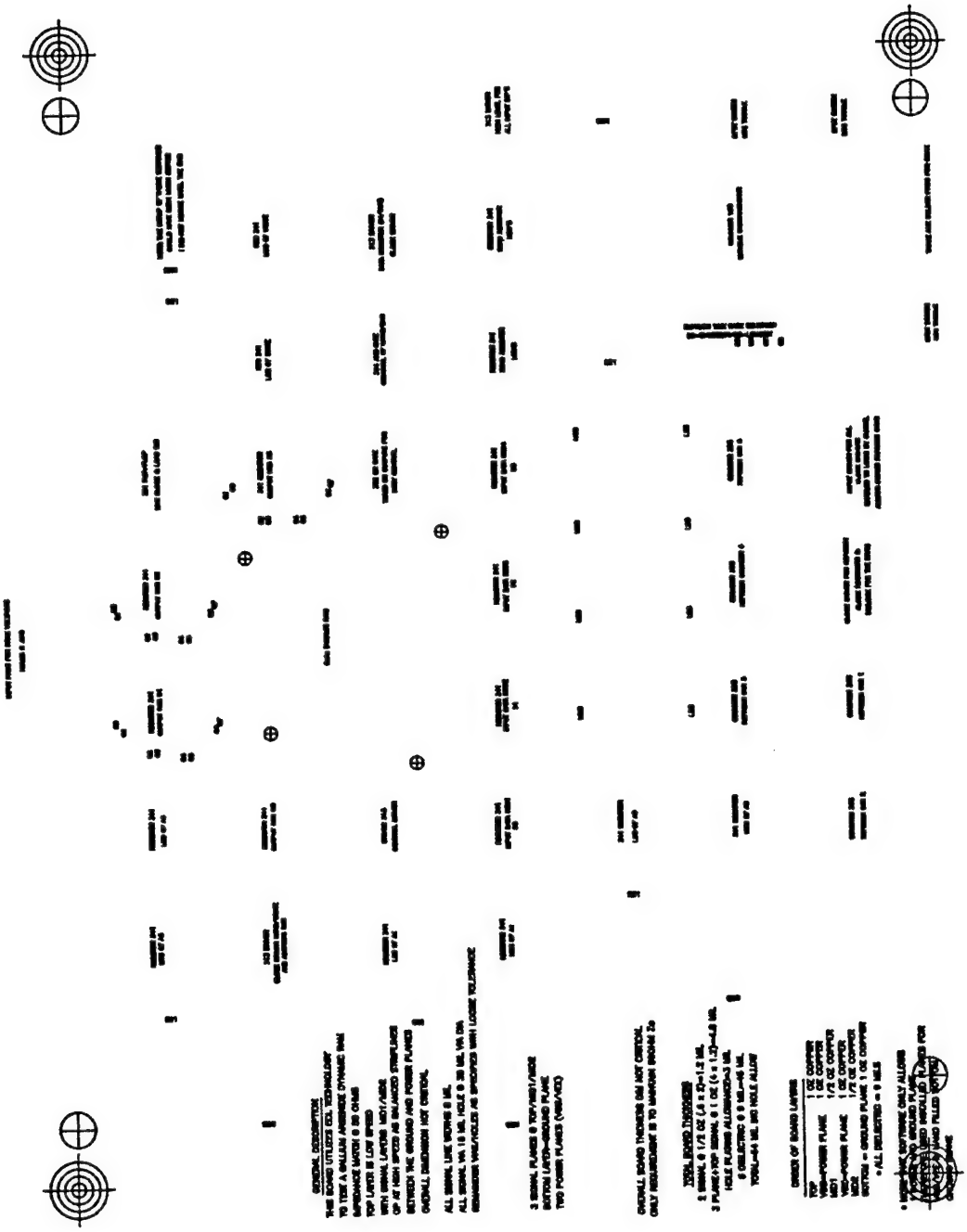

FIGURE A-1 TOP ASSEMBLY LAYER

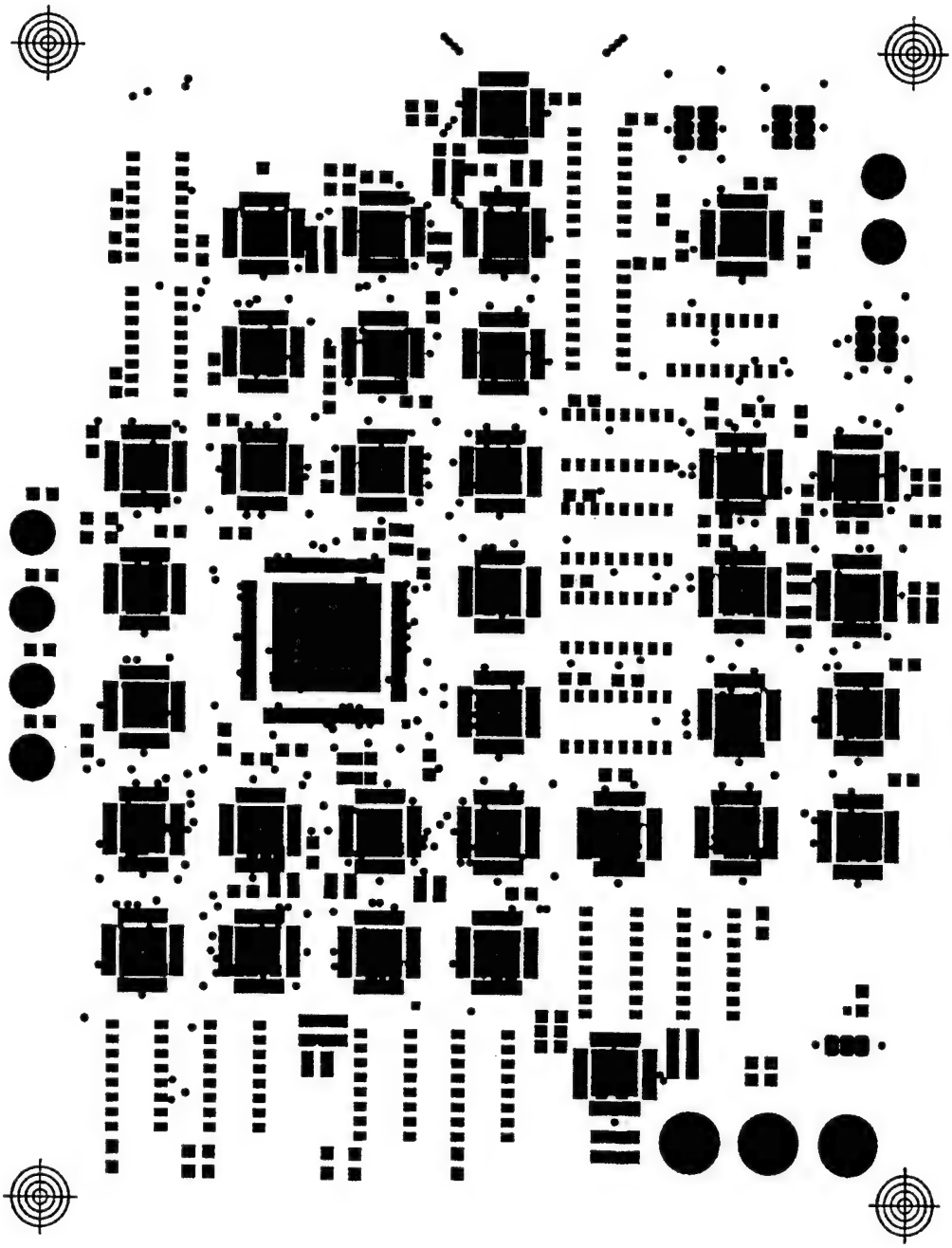

FIGURE A-2 TOP SOLDER MASK

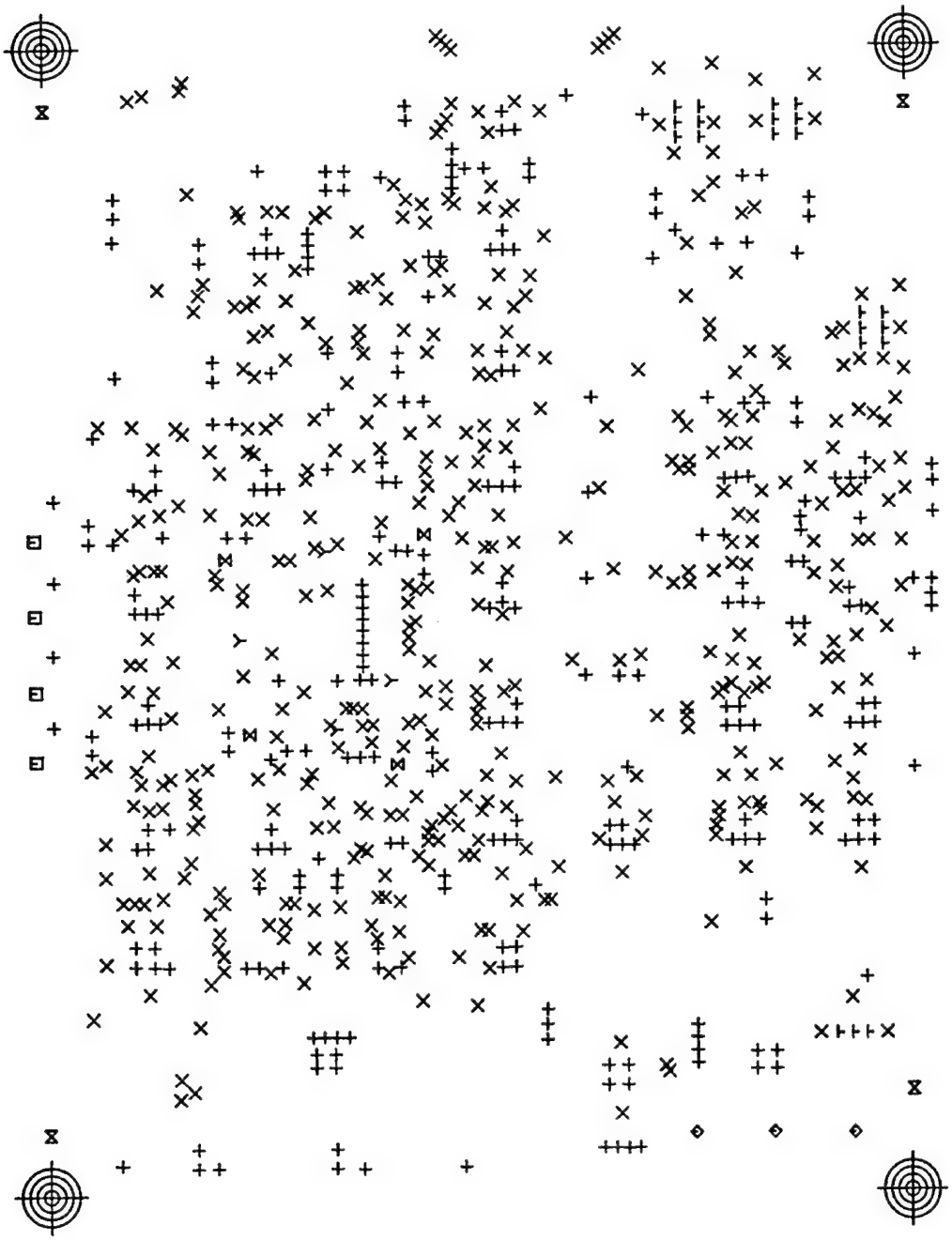

FIGURE A-3 DRILL DRAWING

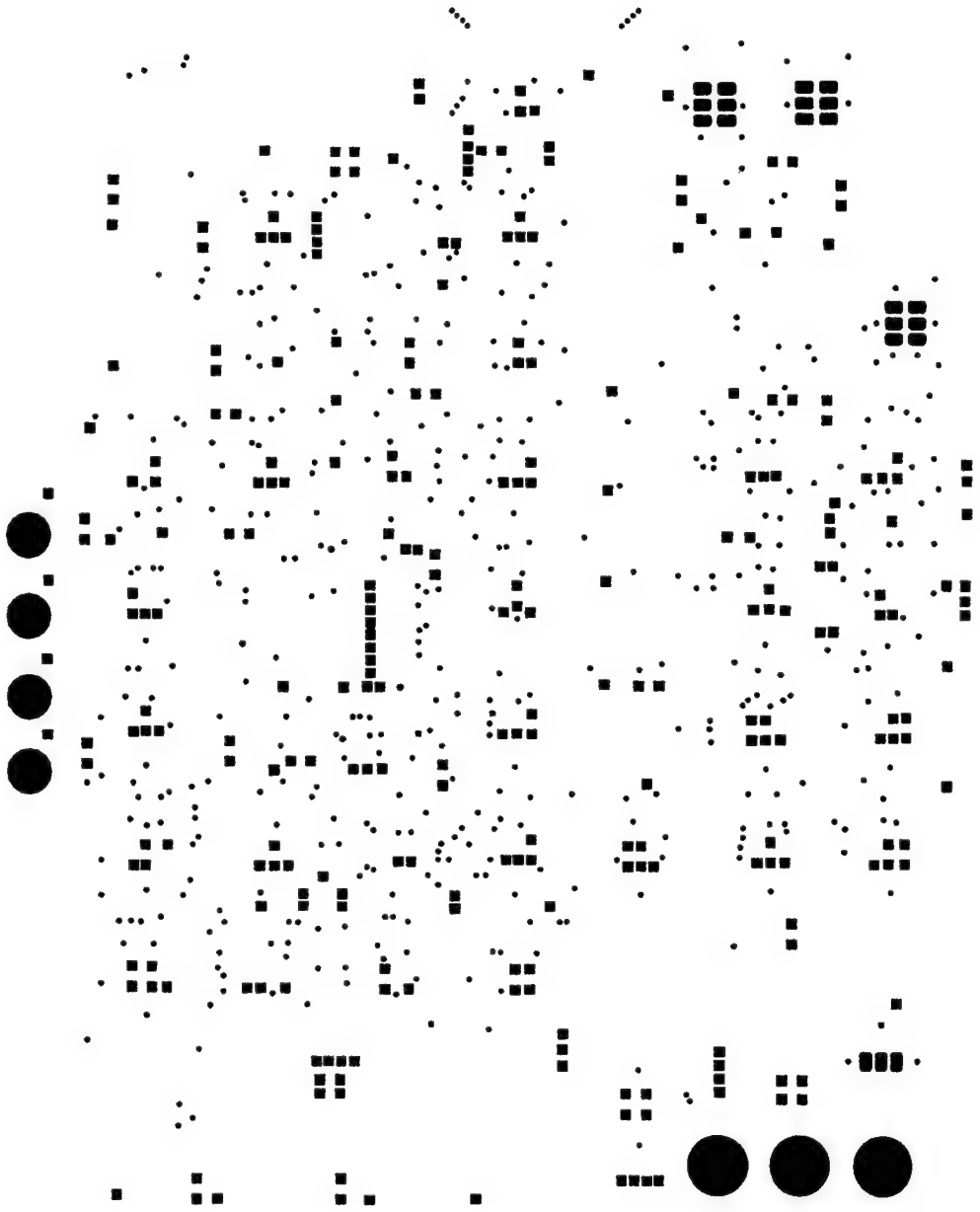

FIGURE A-4 HOLES AND VIAS PLOT

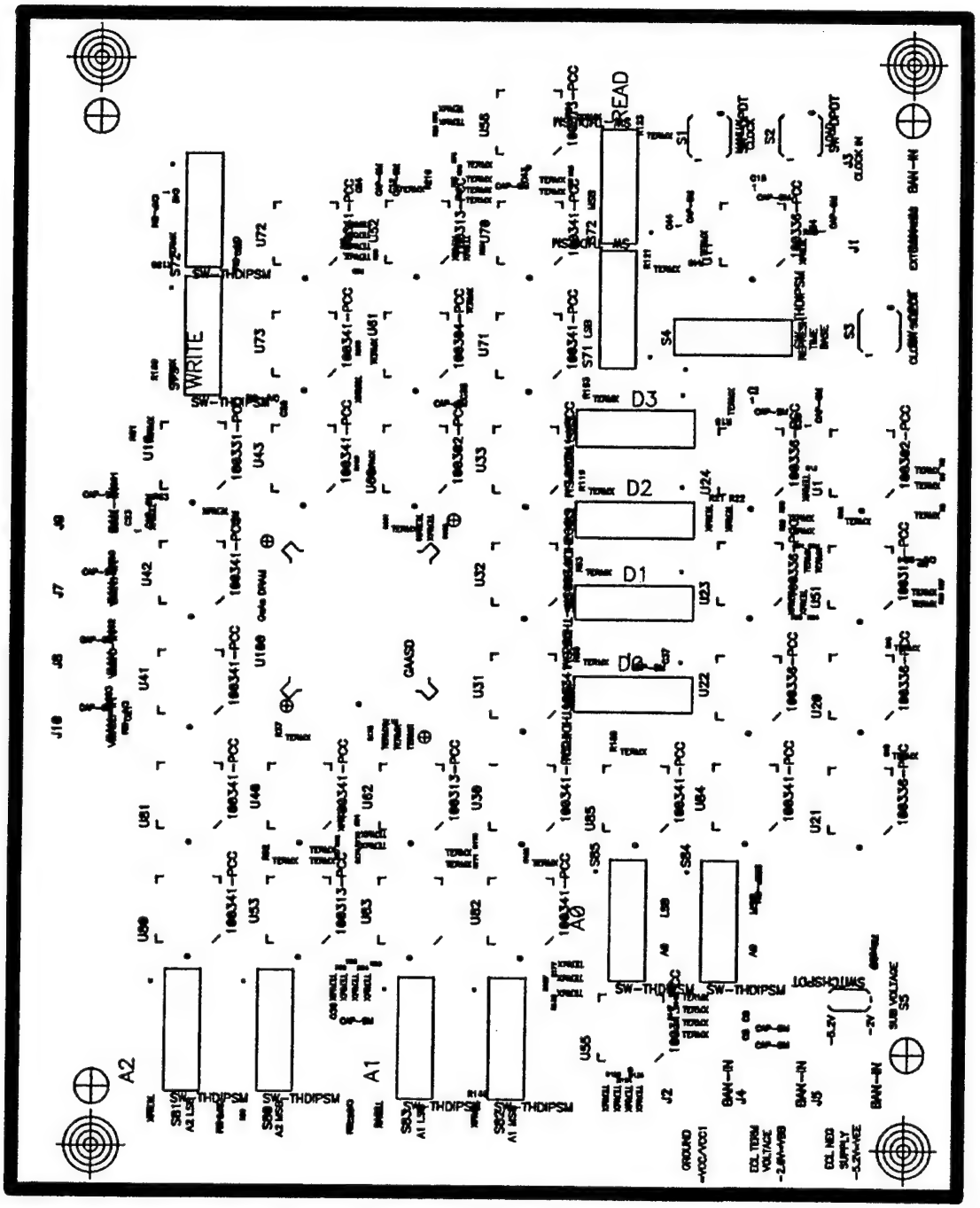

FIGURE A-5 TOP SILK SCREEN LAYER

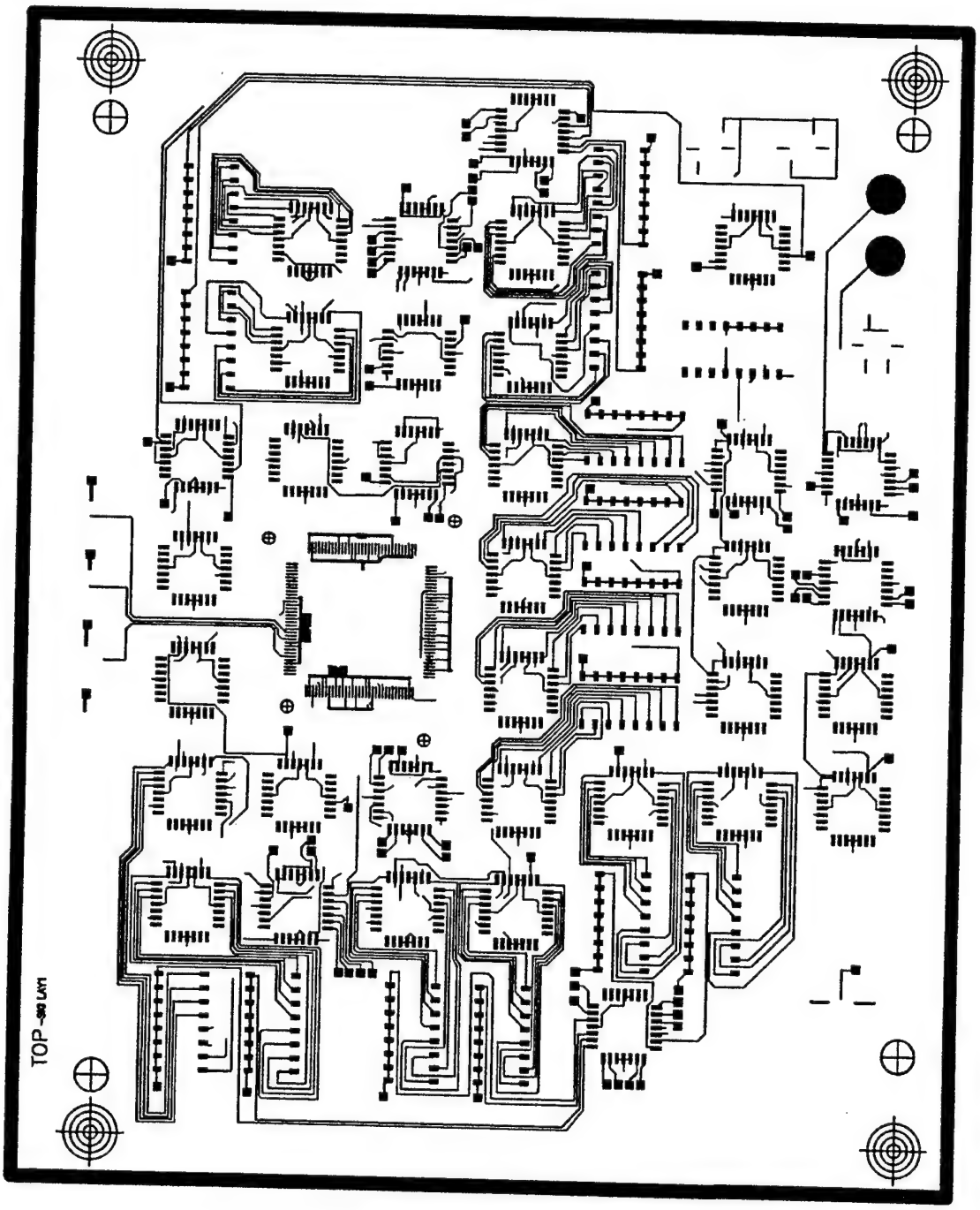

FIGURE A-6 TOP LAYER PADS AND SLOW SPEED SIGNAL

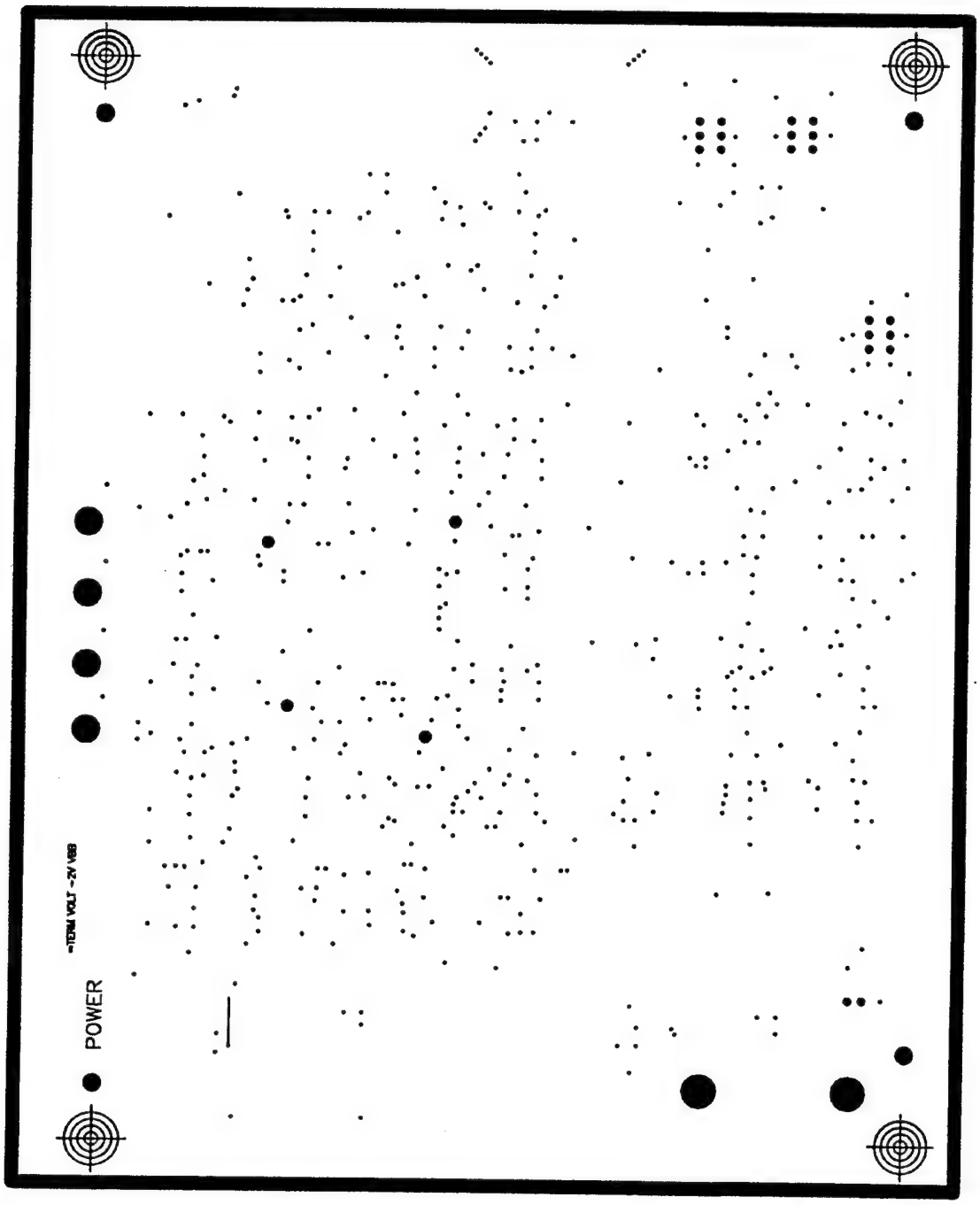

FIGURE A-7 POWER = VBB TERMINATION (NEGATIVE)

FIGURE A-8 LAYER Mid1 = FIRST FAST SIGNAL LAYER

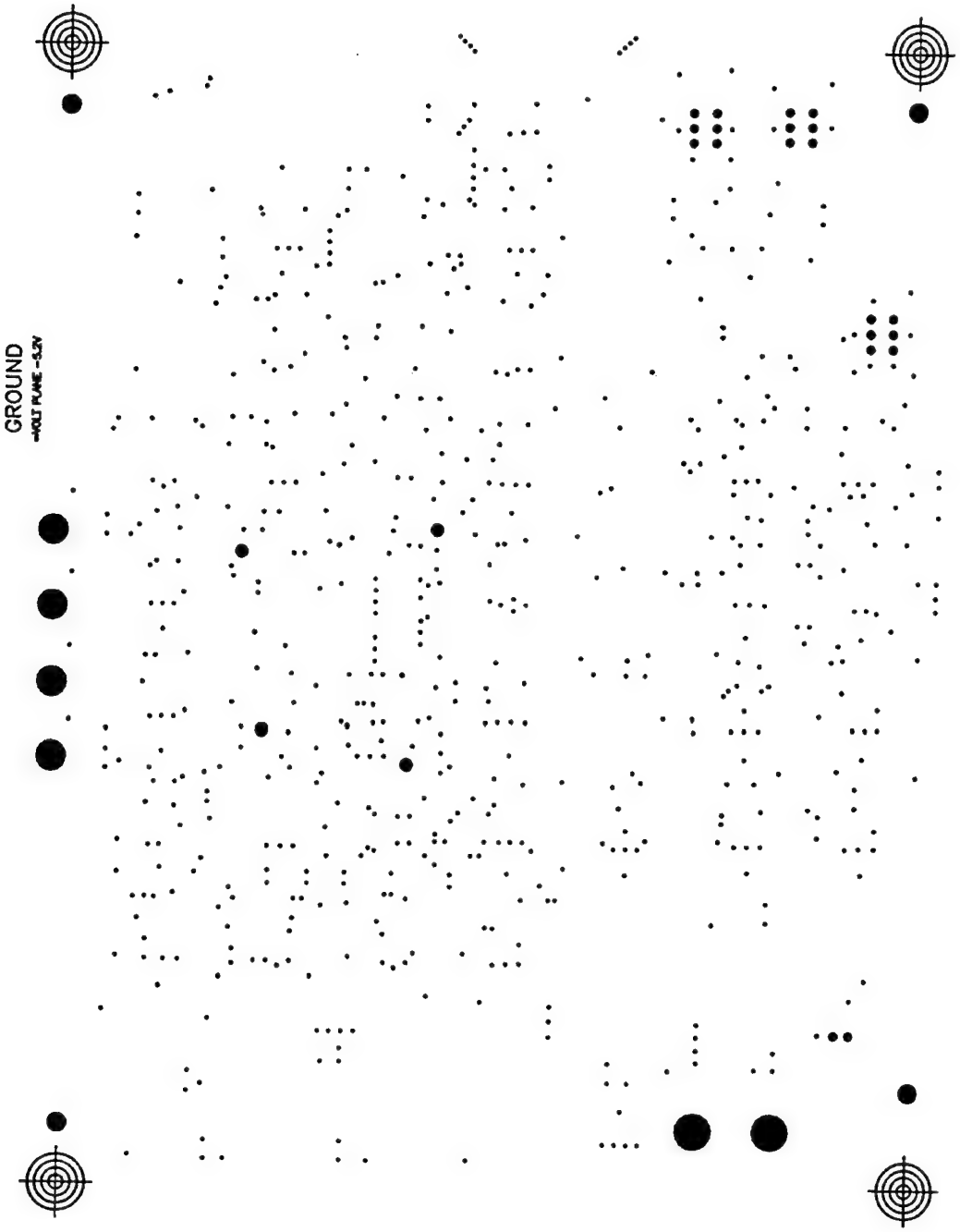

FIGURE A-9 GROUND = VEE LAYER (NEGATIVE)

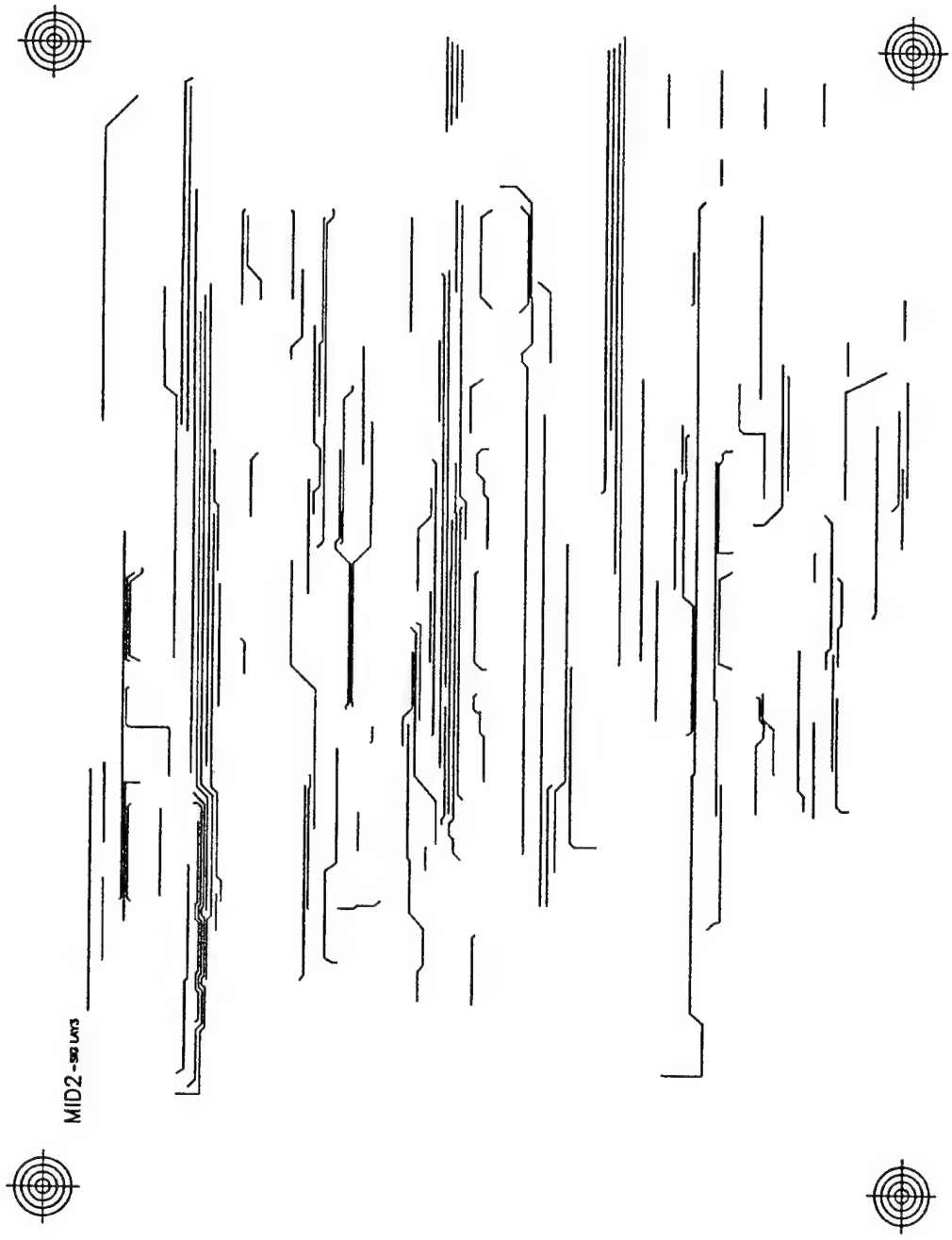

FIGURE A-10 LAYER MID2 = SECOND FAST SIGNAL LAYER

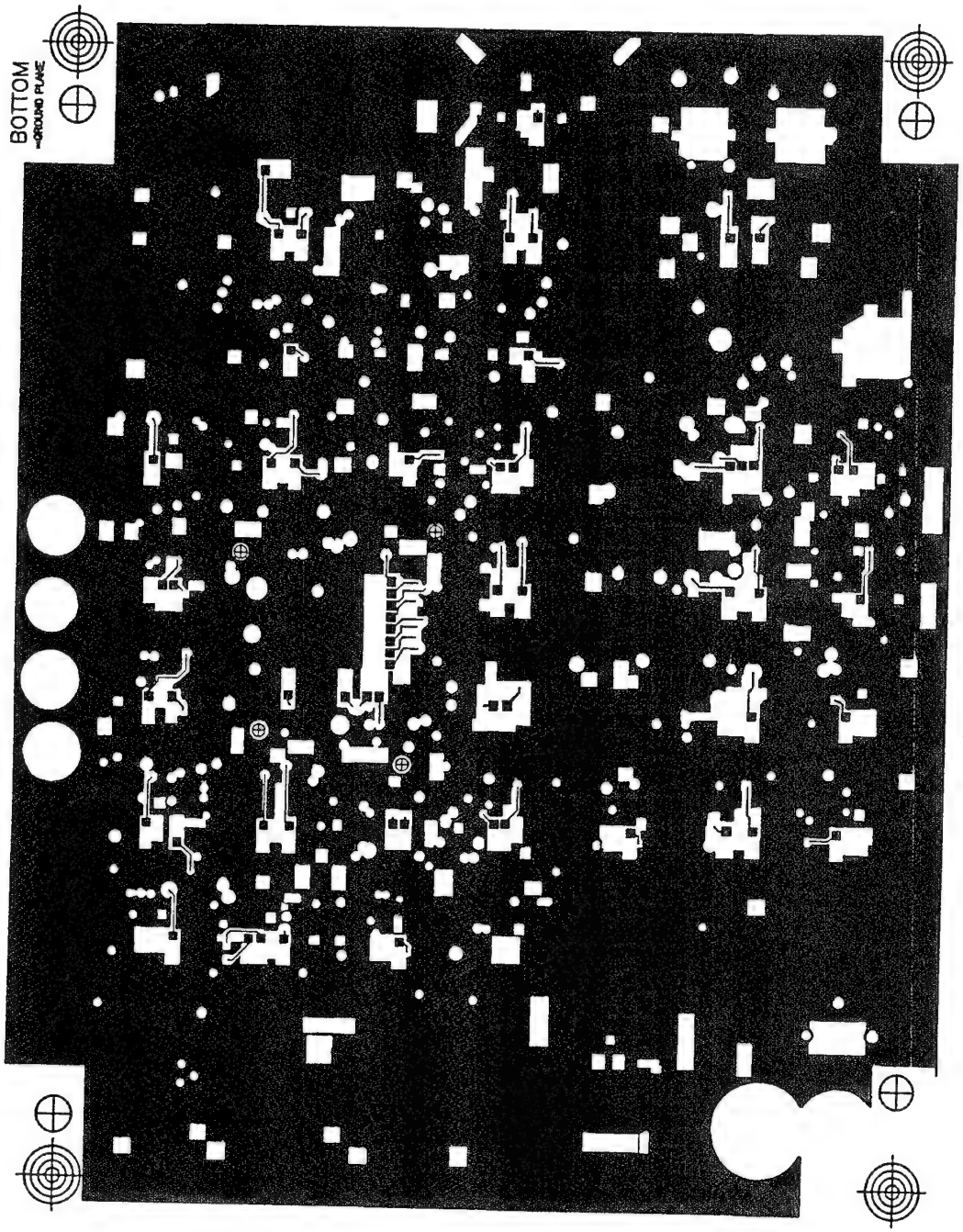

FIGURE A-11 BOTTOM LAYER = TRUE GROUND LAYER

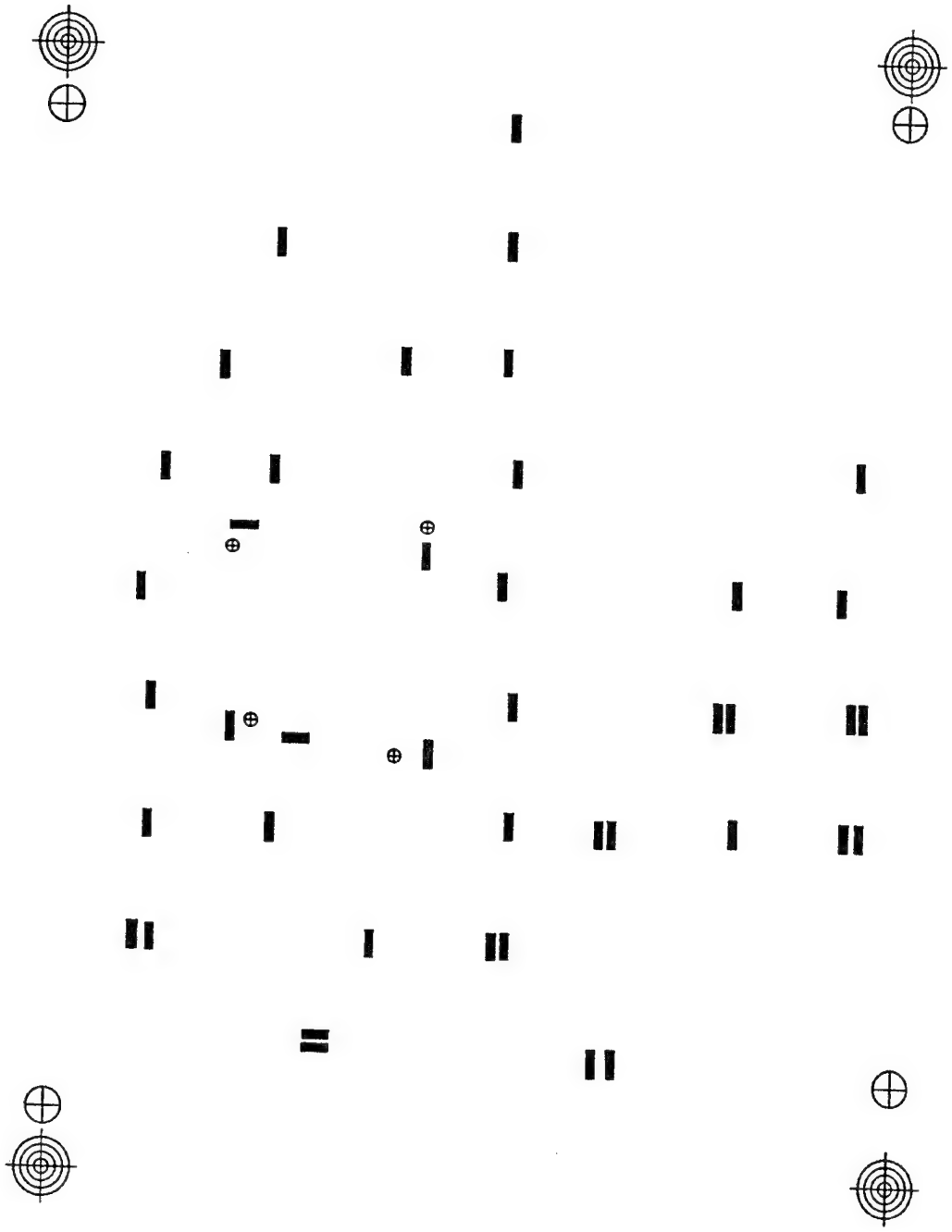

FIGURE A-12 BOTTOM ASSEMBLY LAYER

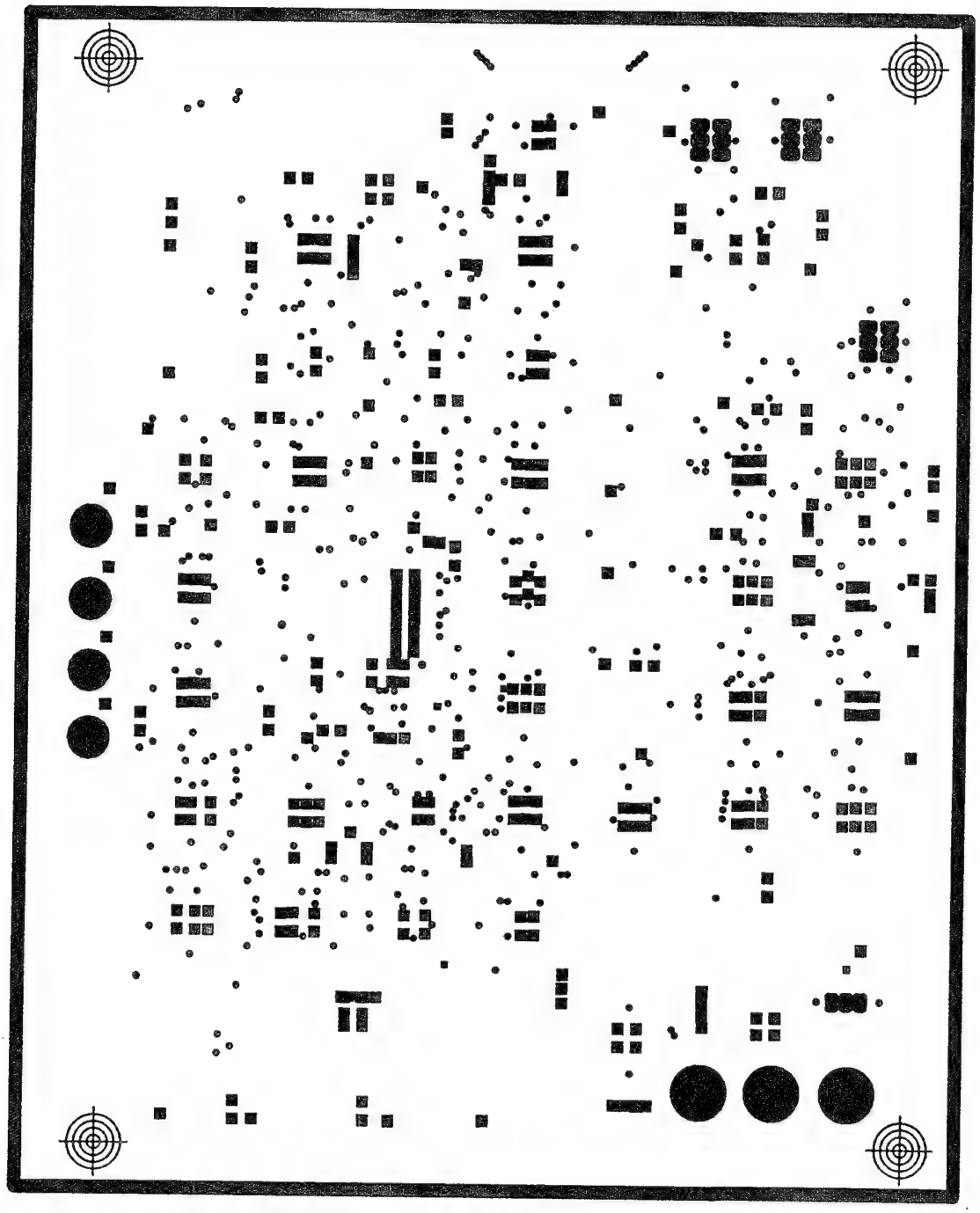

FIGURE A-13 BOTTOM SOLDER MASK

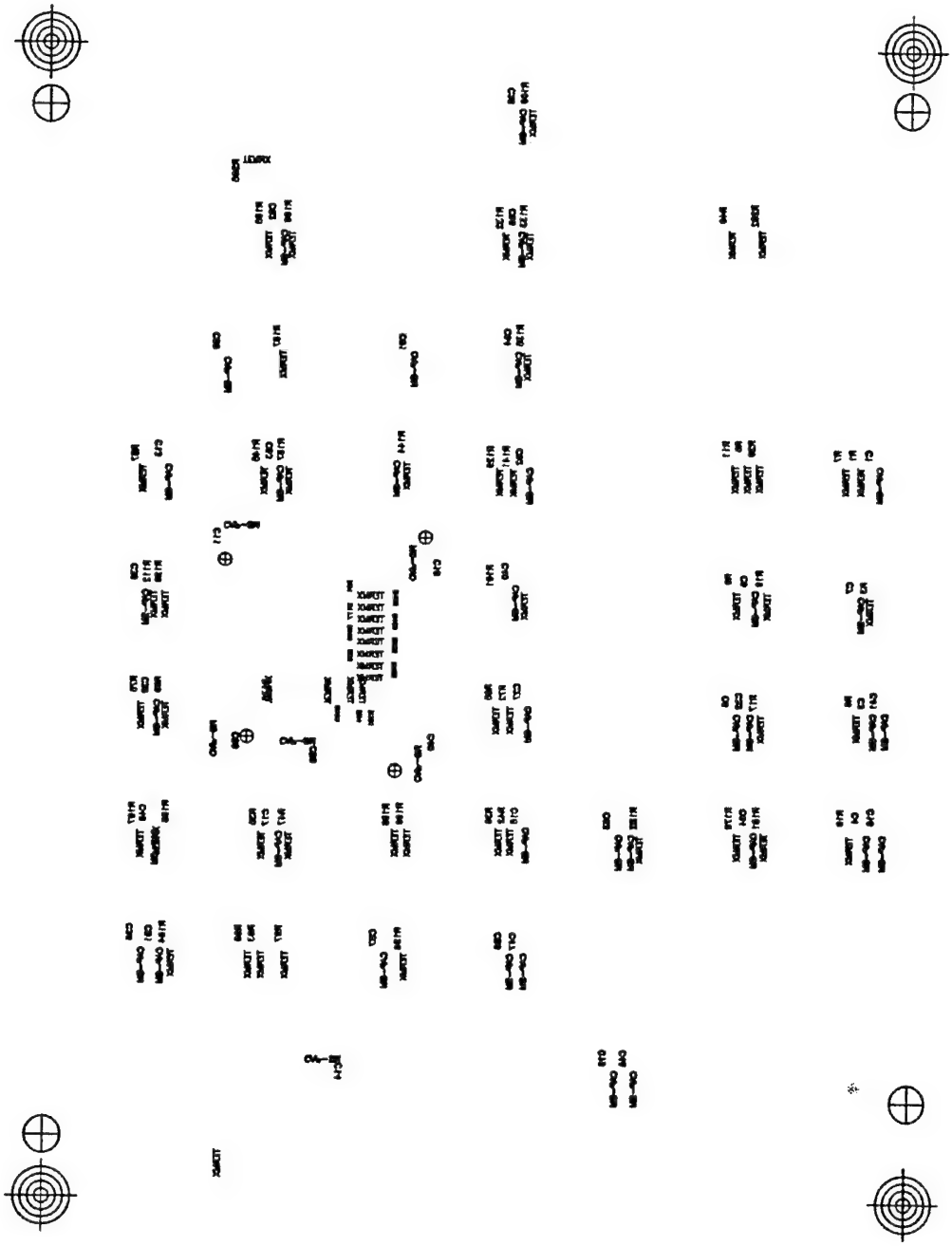

FIGURE A-14 BOTTOM SILK SCREEN

APPENDIX B

A. APERTURE INFORMATION

Aperture Information MOD2.PCB

Aperture and Tool Descriptions

Code	Shape	X	Y	Hole	Type	Comment
D10	Ellipse	008	008	000	Both	Ellipse X_008 Y_008 H_000 FD
D11	Ellipse	010	010	000	Both	Ellipse X_010 Y_010 H_000 FD
D12	Ellipse	012	012	000	Both	Ellipse X_012 Y_012 H_000 FD
D13	Ellipse	020	020	000	Both	Ellipse X_020 Y_020 H_000 FD
D14	Ellipse	100	100	000	Both	Ellipse X_100 Y_100 H_000 FD
D15	Ellipse	040	040	022	Flash	Ellipse X_040 Y_040 H_022 FL
D16	Ellipse	032	032	000	Flash	Ellipse X_032 Y_032 H_000 FL
D17	Ellipse	060	060	000	Flash	Ellipse X_060 Y_060 H_000 FL
D18	Ellipse	300	300	000	Flash	Ellipse X_300 Y_300 H_000 FL
D19	Ellipse	320	320	000	Flash	Ellipse X_320 Y_320 H_000 FL
D20	Ellipse	300	300	200	Flash	Ellipse X_300 Y_300 H_200 FL
D21	Ellipse	210	210	000	Flash	Ellipse X_210 Y_210 H_000 FL
D22	Ellipse	400	400	250	Flash	Ellipse X_400 Y_400 H_250 FL
D23	Ellipse	260	260	000	Flash	Ellipse X_260 Y_260 H_000 FL
D24	Ellipse	420	420	000	Flash	Ellipse X_420 Y_420 H_000 FL
D25	Ellipse	090	090	000	Flash	Ellipse X_090 Y_090 H_000 FL
D26	Ellipse	135	135	000	Flash	Ellipse X_135 Y_135 H_000 FL
D27	Rd Rect	080	120	050	Flash	Rd Rect X_080 Y_120 H_050 FL
D28	Rd Rect	100	140	000	Flash	Rd Rect X_100 Y_140 H_000 FL
D29	Rd Rect	120	080	050	Flash	Rd Rect X_120 Y_080 H_050 FL
D30	Rd Rect	140	100	000	Flash	Rd Rect X_140 Y_100 H_000 FL
D31	Sq Rect	012	060	000	Flash	Sq Rect X_012 Y_060 H_000 FL
D32	Sq Rect	032	080	000	Flash	Sq Rect X_032 Y_080 H_000 FL
D33	Sq Rect	012	076	000	Flash	Sq Rect X_012 Y_076 H_000 FL
D34	Sq Rect	032	096	000	Flash	Sq Rect X_032 Y_096 H_000 FL
D35	Sq Rect	012	080	000	Flash	Sq Rect X_012 Y_080 H_000 FL
D36	Sq Rect	032	100	000	Flash	Sq Rect X_032 Y_100 H_000 FL
D37	Sq Rect	012	082	000	Flash	Sq Rect X_012 Y_082 H_000 FL
D38	Sq Rect	032	102	000	Flash	Sq Rect X_032 Y_102 H_000 FL
D39	Sq Rect	012	084	000	Flash	Sq Rect X_012 Y_084 H_000 FL
D40	Sq Rect	032	104	000	Flash	Sq Rect X_032 Y_104 H_000 FL
D41	Sq Rect	026	080	000	Flash	Sq Rect X_026 Y_080 H_000 FL
D42	Sq Rect	046	100	000	Flash	Sq Rect X_046 Y_100 H_000 FL
D43	Sq Rect	036	066	000	Flash	Sq Rect X_036 Y_066 H_000 FL
D44	Sq Rect	056	086	000	Flash	Sq Rect X_056 Y_086 H_000 FL
D45	Sq Rect	064	064	000	Flash	Sq Rect X_064 Y_064 H_000 FL

Code	Shape	X	Y	Hole	Type	Comment
D46	Sq Rect	084	084	000	Flash	Sq Rect X_084 Y_084 H_000 FL
D47	Sq Rect	064	064	015	Flash	Sq Rect X_064 Y_064 H_015 FL
D48	Ellipse	025	025	000	Flash	Ellipse X_025 Y_025 H_000 FL
D49	Sq Rect	066	036	000	Flash	Sq Rect X_066 Y_036 H_000 FL
D50	Sq Rect	086	056	000	Flash	Sq Rect X_086 Y_056 H_000 FL
D51	Sq Rect	072	012	000	Flash	Sq Rect X_072 Y_012 H_000 FL
D52	Sq Rect	092	032	000	Flash	Sq Rect X_092 Y_032 H_000 FL
D53	Sq Rect	080	026	000	Flash	Sq Rect X_080 Y_026 H_000 FL
D54	Sq Rect	100	046	000	Flash	Sq Rect X_100 Y_046 H_000 FL
D55	Sq Rect	084	012	000	Flash	Sq Rect X_084 Y_012 H_000 FL
D56	Sq Rect	104	032	000	Flash	Sq Rect X_104 Y_032 H_000 FL
D57	Ellipse	032	032	016	Flash	Ellipse X_032 Y_032 H_016 FL
D58	Ellipse	026	026	000	Flash	Ellipse X_026 Y_026 H_000 FL
D59	Ellipse	052	052	000	Flash	Ellipse X_052 Y_052 H_000 FL
D60	Sq Rect	032	032	016	Flash	Sq Rect X_032 Y_032 H_016 FL
D61	Sq Rect	052	052	000	Flash	Sq Rect X_052 Y_052 H_000 FL

Code	Hole Diameter
T01	015
T02	016
T03	022
T04	050
T05	080
T06	125
T07	200
T08	250

B. TOOL ASSIGNMENTS

Aperture Information MOD2.PCB

Aperture and Tool Assignments

Item	Normal	S Mask	Plane	Thermal	Drl Sym	Tool
DRAW APERTURE	D10	-	-	-	-	-
LINE_008	D10	-	-	-	-	-
LINE_010	D11	-	-	-	-	-
LINE_012	D12	-	-	-	-	-
LINE_020	D13	-	-	-	-	-
LINE_100	D14	-	-	-	-	-
P_EL_0040_0040_022_AL	D15	D17	D16	DRAW	-	-
P_EL_0300_0300_000_TL	D18	D19	-	-	-	-
P_EL_0300_0300_200_AL	D20	D19	D21	DRAW	-	-
P_EL_0400_0400_250_AL	D22	D24	D23	DRAW	-	-
P_MH_0090_0090_080_AL	DRAW	-	D25	-	-	-
P_MH_0250_0250_125_AL	DRAW	-	D26	-	-	-
P_RR_0080_0120_050_AL	D27	D28	D17	DRAW	-	-
P_RR_0120_0080_050_AL	D29	D30	D17	DRAW	-	-
P_SQ_0012_0060_000_TL	D31	D32	-	-	-	-
P_SQ_0012_0076_000_TL	D33	D34	-	-	-	-
P_SQ_0012_0080_000_TL	D35	D36	-	-	-	-
P_SQ_0012_0082_000_TL	D37	D38	-	-	-	-
P_SQ_0012_0084_000_TL	D39	D40	-	-	-	-
P_SQ_0026_0080_000_TL	D41	D42	-	-	-	-
P_SQ_0036_0066_000_TL	D43	D44	-	-	-	-
P_SQ_0064_0064_000_BL	D45	D46	-	-	-	-
P_SQ_0064_0064_000_TL	D45	D46	-	-	-	-
P_SQ_0064_0064_015_AL	D47	D46	D48	DRAW	-	-
P_SQ_0066_0036_000_TL	D49	D50	-	-	-	-
P_SQ_0072_0012_000_TL	D51	D52	-	-	-	-
P_SQ_0080_0026_000_TL	D53	D54	-	-	-	-
P_SQ_0084_0012_000_TL	D55	D56	-	-	-	-
P_TG_0500_0500_000_AL	DRAW	-	-	-	-	-
V_CR_032_016	D57	D59	D58	DRAW	-	-
V_SQ_032_016	D60	D61	D58	DRAW	-	-
HOLE_015	-	-	-	-	DRAW	T01
HOLE_016	-	-	-	-	DRAW	T02
HOLE_022	-	-	-	-	DRAW	T03
HOLE_050	-	-	-	-	DRAW	T04
HOLE_080	-	-	-	-	DRAW	T05
HOLE_125	-	-	-	-	DRAW	T06
HOLE_200	-	-	-	-	DRAW	T07
HOLE_250	-	-	-	-	DRAW	T08

- : Not applicable. * : Aperture/tool is not assigned.

C. BILL OF MATERIALS

Bill of Materials MOD2.PCB

Quantity	Type	Value	Ref Designators
1	100302-PCC		U60
1	100302-PCC	VAL	U1
1	100304-PCC	VAL	U61
1	100313-PCC		U62
5	100313-PCC	VAL	U51,U52,U53,U55,U56
1	100331-PCC	VAL	U10
4	100336-PCC		U21,U22,U23,U24
2	100336-PCC	VAL	U11,U20
17	100341-PCC		U31,U32,U33,U40,U41,U42, U43,U70,U71,U72,U73,U80, U81,U82,U83,U84,U85
1	100341-PCC	VAL	U30
1	BAN-IN	CLOCK	J3
1	BAN-IN	GND	J2
1	BAN-IN	REFRESH-OPT	J1
1	BAN-IN	VBB	J4
1	BAN-IN	VEE	J5
1	BAN-IN	VREFB	J7
1	BAN-IN	VREFD	J8
1	BAN-IN	VRVREF	J10
1	BAN-IN	VSS	J9
69	CAP-SM	VAL	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C31,C32, C33,C34,C35,C36,C37,C38, C39,C40,C41,C42,C43,C44, C45,C46,C47,C48,C49,C50, C51,C52,C53,C54,C55,C56, C57,C58,C59,C60,C61,C62, C63,C64,C200,C201,C202, C203,C204
1	GAASD	VAL	U100
3	SW-DPDT	VAL	S1,S2,S3
15	SW-THDIPSM	VAL	S4,S30,S31,S32,S33,S70, S71,S72,S73,S80,S81,S82, S83,S84,S85
1	SWITCHSPDT	VAL	S5
137	TERMX		R2,R4,R5,R6,R8,R9,R10,R11, R12,R13,R15,R16,R17,R18, R19,R20,R21,R22,R29,R30, R35,R36,R37,R38,R39,R40,

Quantity	Type	Value	Ref Designators
			R41,R42,R44,R46,R47,R49, R53,R55,R58,R59,R60,R62, R64,R65,R66,R67,R68,R70, R72,R74,R75,R78,R80,R81, R83,R84,R86,R87,R88,R89, R90,R91,R92,R93,R94,R95, R96,R97,R98,R99,R100,R101, R102,R103,R104,R105,R106, R107,R108,R109,R112,R117, R119,R120,R121,R123,R124, R125,R126,R127,R128,R129, R130,R131,R132,R133,R134, R135,R136,R137,R139,R140, R141,R143,R144,R145,R147, R149,R153,R155,R156,R157, R159,R160,R161,R162,R163, R165,R166,R167,R168,R169, R170,R171,R172,R173,R174, R175,R176,R177,R178,R179, R180,R181,R182,R183,R184, R185,R202,R205,R210
12	TERMX	VAL	R1,R3,R7,R23,R24,R25,R27, R28,R51,R57,R63,R158
1	TERMX	VEE	R26

D. PCB STATISTICS

PCB Statistics MOD2.PCB

Arcs:	329	Components:	282	Pads:	1808	Polygons:	604
Lines:	6014	Text strings:	816	Vias:	464	Holes:	787

Text Summary -

T_0028_008_0:	176
T_0028_008_1:	15
T_0028_008_3:	13
T_0028_008_4:	11
T_0040_008_0:	88
T_0040_008_1:	16
T_0040_008_2:	26
T_0040_008_3:	45
T_0040_008_4:	106
T_0040_008_5:	1
T_0040_008_6:	5
T_0040_008_7:	8
T_0040_010_0:	22
T_0040_010_1:	2
T_0040_010_2:	7
T_0040_010_3:	14
T_0040_010_4:	70
T_0040_010_5:	3
T_0040_010_6:	3
T_0048_008_0:	45
T_0060_010_0:	92
T_0060_010_1:	3
T_0060_010_2:	4
T_0060_010_3:	8
T_0060_012_0:	18
T_0100_008_0:	11
T_0100_008_3:	4

Line Summary -

L_008:	5086
L_010:	641
L_012:	498
L_020:	114
L_100:	4

Pad Summary -

P_EL_0040_0040_022_AL:	4
P_EL_0300_0300_000_TL:	2
P_EL_0300_0300_200_AL:	4
P_EL_0400_0400_250_AL:	3
P_MH_0090_0090_080_AL:	4
P_MH_0250_0250_125_AL:	4

	P_RR_0080_0120_050_AL:	18
	P_RR_0120_0080_050_AL:	3
	P_SQ_0012_0060_000_TL:	2
	P_SQ_0012_0076_000_TL:	1
	P_SQ_0012_0080_000_TL:	1
	P_SQ_0012_0082_000_TL:	1
	P_SQ_0012_0084_000_TL:	61
	P_SQ_0026_0080_000_TL:	476
	P_SQ_0036_0066_000_TL:	160
	P_SQ_0064_0064_000_BL:	63
	P_SQ_0064_0064_000_TL:	92
	P_SQ_0064_0064_015_AL:	283
	P_SQ_0066_0036_000_TL:	80
	P_SQ_0072_0012_000_TL:	7
	P_SQ_0080_0026_000_TL:	476
	P_SQ_0084_0012_000_TL:	59
	P_TG_0500_0500_000_AL:	4
Via Summary -	V_CR_032_016:	460
	V_SQ_032_016:	4
Hole Summary -	H_015:	283
	H_016:	464
	H_022:	4
	H_050:	21
	H_080:	4
	H_125:	4
	H_200:	4
	H_250:	3
Plane Connections -	Power Thermals:	0
	Power Directs:	186
	Ground Thermals:	0
	Ground Directs:	100

E. DESIGN RULE CHECK

Design Rule Check Report MOD2.PCB

DRC Clearances (in mils)

	Top	Bot	Mid1	Mid2	Mid3	Mid4	Mid5	Mid6	Mid7	Mid8
Pad-to-Pad	8	8	8	8	8	8	8	8	8	8
Pad-to-Line	8	8	8	8	8	8	8	8	8	8
Line-to-Line	8	8	8	8	8	8	8	8	8	8
Hole-to-Hole	8									

DRC Report Options

Clearance Violations:	enabled
Text Violations:	disabled
Net List Violations:	enabled
Single Node Routes:	enabled
Unconnected Pins:	disabled
Unplaced Nodes:	disabled

DRC Errors

DRC Summary

0 errors detected

APPENDIX C

This section contains the READ.ME file that was sent to the fabrication house with the final photo plot files for manufacturing the PCB.

West Coast Circuits, Inc.
1080 West Beach St.
Watsonville, California 95076
BUS: (408) 728-4271
FAX: (408) 728-1827

ATTRIBUTE DESCRIPTION		VALUE	NOTES
Technology		SURFACE MOUNT	
Dimensions	Width	8.5 in.	
	Depth	7 in.	
	Thickness	71_3 mils	*6 mil for hole plating
	Board Material	FR4	
Layers			
1. Low Speed Signal/Surface		1 mil thick	1 oz copper
2. Voltage Plane VBB termination		1 mil thick	1 oz copper
3. High-Speed Signal (Mid1)		1 mil thick	1 oz copper
4. Voltage Plane VEE		1 mil thick	1 oz copper
5. High-Speed Signal(Mid2)		1 mil thick	1 oz copper

	6. Bottom Voltage Plane (GND)	1 mil thick	1 oz copper
	7. Dielectric Thickness	13 mil	5 layers
Components	34 28-pin PLCC IC's		300 Series ECL National Semiconductor
	Resistors (termination)		150 surface mount 1206
	Capacitors(bypass)		69 surface mount 1206
	1 132-pin PLCC		GaAs DRAM
	4 switches		
	15 eight position dip		surface mount
Line Width	All signals		8 mil
Total Lines	Signal + Bottom Plane Fill		8-10-12-20-100 >5000 line segments
Total Vias	Includes Vias+GND Plane Conn		464 vias 32 milx 16 mil hole or larger
Total Holes	Vias+ThruPads to Planes		780 hole clearance @ 30 mils
VBB Connect	Connections to VBB Plane		186 resistors + bypass caps
VEE Connect	Connection to VEE Plane		100 bypass caps+chip power
Design Rules	Clearance Pad to Pad		8 mil
	Clearance Pad to Line		8 mil
	Clearance Line to Line		8 mil
	Clearance Hole to Hole		30 mil

Solder Mask PC401

The board is made to have alternating signal and ground plane layers with striplines running between the planes. Note that both the POWER (VBB termination voltage) and GROUND (VEE reference voltage) planes are plotted in the negative due to the software constraints. The BOTTOM layer which is the true GROUND plane is plotted in positive. The layers are labeled in order of their position as follows:

	LAYER	MASK POLARITY
*	TOP ASSEMBLY LAYER	Positive
*	TOP SOLDER MASK	Positive
*	DRILL DRAWING	Positive
*	HOLES AND VIAS PLOT	Positive
*	TOP SILK SCREEN	Positive
*	TOP LAYER PADS AND SLOW SPEED SIGNAL	Positive
*	GROUND=VEE LAYER	Negative
*	LAYER Mid1=FIRST FAST SIGNAL LAYER	Positive
*	POWER=VBB TERMINATION VOLTAGE	Negative
*	LAYER MID2=SECOND FAST SIGNAL LAYER	Positive
*	BOTTOM LAYER=TRUE GROUND PLANE	Positive
*	BOTTOM ASSEMBLY LAYER	Positive
*	BOTTOM SOLDER MASK	Positive
*	BOTTOM SILK SCREEN	Positive

APPENDIX D

This section contains the high reliability soldering techniques used in the assembly of the PCB.

A. PREPARATION

- Clean pads, component leads, and solder with residue free alcohol.
- If pads or leads are heavily corroded use gun eraser to remove corrosion.
- Clean soldering iron tip by repeated passes over lint free cloth or tissue.
- Ensure soldering iron is well tinned.
- If possible, pre-tin component leads to ensure good solder flow.
- Use 63/37 solder for best flow, electrical and mechanical characteristics.

B. SOLDERING

- Use 45 watt or 700°F soldering iron.
- Use a heat sink (forceps or alligator clips) to prevent component damage.
- Apply soldering iron to the lead and pad simultaneously.
- Use only enough solder to obtain a convex shape around the lead and flowing out to the edges of the pad.
- Immediately after removing heat, 'quench' the solder connection with alcohol using a short stiff bristle brush.

C. CLEAN UP AND INSPECTION

- Clean the solder joint with a short stiff bristle brush with alcohol to remove all flux.

- Dry and polish the joint using cotton tipped cleaning sticks with a circular motion around the joint ("twirling the stick").

- Inspect the joint for any of the following defects which could indicate a cold solder joint:

- Dull finish.

- Wavy lines in the solder.

- Pitted areas in the solder.

- Partial solder flow on lead or pad.

LIST OF REFERENCES

1. Morris, Michael A., *A GaAs DRAM*, Master's Thesis, Naval Postgraduate School, Monterey, California, December 1992.

2. Butler, Michael P., *Test Methods and Custom Hardware for Functional Testing of a High-Speed GaAs DRAM*, Master's Thesis, Naval Postgraduate School, Monterey, California, September 1993.

3. ACCEL Technologies, Inc., *TANGO PCB-PLUS*, ver 2.1.

4. Blood, William Jr., *MECL System Design Handbook*, Motorola Semiconductor Products Inc, 1988.

5. Autodesk, Inc., *AutoCAD, Release 11*.

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